BAB VI

KESIMPULAN

6.1. Kesimpulan

Berdasarkan hasil pembahasan yang telah dilakukan, maka kesimpulan yang dapat ditarik dari penelitian ini adalah:

- Panjang langkah gerak robot
  - o Buka-tutup *gripper* : 30 mm
  - o Atas-bawah lengan : 180 mm
  - o Kanan-kiri lengan : 180°
  - o Maju-mundur lengan : 100 mm
- Beban maksimum
  - o Genggaman *gripper* : 200 gram
  - o Angkatan lengan : 250 gram
- Daya genggam dan angkat dipengaruhi oleh torsi motor DC 12 Volt
- Kecepatan gerak robot
  - o Tanpa beban
    - Membuka *gripper* : 10 mm/s
    - Menutup *gripper* : 10 mm/s
    - Lengan bergerak ke atas : 10 mm/s
    - Lengan bergerak ke bawah : 10 mm/s
    - Lengan bergerak ke kiri : 20°/s
    - Lengan bergerak ke kanan : 20°/s
    - Lengan bergerak maju : 10 mm/s
    - Lengan bergerak mundur : 10 mm/s

- Dengan beban
  - Membuka *gripper* : 10 mm/s
  - Menutup *gripper* : 10 mm/s
  - Lengan bergerak ke atas : 7,5 mm/s
  - Lengan bergerak ke bawah : 9 mm/s
  - Lengan bergerak ke kiri : 18°/s
  - Lengan bergerak ke kanan : 18°/s
  - Lengan bergerak maju : 8,3 mm/s
  - Lengan bergerak mundur : 8,3 mm/s

- Motor DC 12 Volt akan menyerap arus yang lebih besar jika diberi beban dan akan berhenti pada batas kemampuannya
- Jangkauan *counter*
  - Gerak tutup-buka *gripper* : 40 *clock*
  - Gerak naik-turun lengan : 180 *clock*
  - Gerak maju-mundur lengan : 100 *clock*
  - Gerak kanan-kiri lengan : 144 *clock*
- Analisis data kepresisian *counter* target terhadap *counter* hasil
  - Rata-rata penyimpangan : 1,2 *clock*
  - *Range*/jangkauan penyimpangan : 3 *clock*
  - Deviasi standar penyimpangan : 0,78
  - Koefisien σ penyimpangan : 65%
- Rata-rata penyimpangan akan terus bertambah sesuai dengan panjang langkah gerak robot
- Kepresisian ditentukan oleh penggunaan *limit switch*
- Penggantian koordinat *point* dilakukan dengan mengubah program
- Penggantian program atau kode tidak perlu dengan melepas dan memasang *chip* mikrokontroler

6.2. Saran

Dari penelitian ini, penulis mengajukan beberapa saran agar penelitian mendatang lebih baik. Saran-saran tersebut adalah:

a) Meningkatkan kepresisian panjang langkah gerakan robot dengan penggunaan motor *stepper*.
b) Menggunakan sensor *infra red* untuk meningkatkan keakurasian *counter clock*.
c) Memperhitungkan *repeatability* dan akurasi gerak robot.

DAFTAR PUSTAKA

Blocher, R., 2003, *Dasar Elektronika*, Andi, Yogyakarta

Bateson, W., 1999, *Input and Output Device,* Prentice Hall, New Jersey

Groover, M., 1987, *Automation, Production Systems and Computer-Integrated Manufacturing,* Prentice Hall, New Jersey

Maystel, A., 1991, *Autonomous Mobile Robots Vehicles with Cognitive Control,* World Scientific, Singapore

Nurdinsidiq, M dan Sutopo, B, 2001, *Pengendalian Lengan Robot Berbasis Mikrokontroler AT89C51 Menggunakan Transduser Ultrasonik*, Jurnal Teknik Elektronika, Universitas Gajah Mada, Yogyakarta

Putra, A.E., 2004, *Belajar Mikrokontroler AT89C51 Teori dan Aplikasi*, II, Gava Media, Yogyakarta

Steward, J.W., Miao, K.X., 1999, *The 8051 Microcontroler: Hardware, Software and Interfacing*, II, Prentice Hall, New Jersey

Waugh, A.E., 1952, Elemen dari Metode Statistika, Andi, Yogyakarta

LAMPIRAN 1

Data Sheet
Mikrokontroler AT89C51

Features

- Compatible with MCS-51™ Products
- 4K Bytes of In-System Reprogrammable Flash Memory
  - Endurance: 1,000 Write/Erase Cycles
- Fully Static Operation: 0 Hz to 24 MHz
- Three-level Program Memory Lock
- 128 x 8-bit Internal RAM
- 32 Programmable I/O Lines
- Two 16-bit Timer/Counters
- Six Interrupt Sources
- Programmable Serial Channel
- Low-power Idle and Power-down Modes

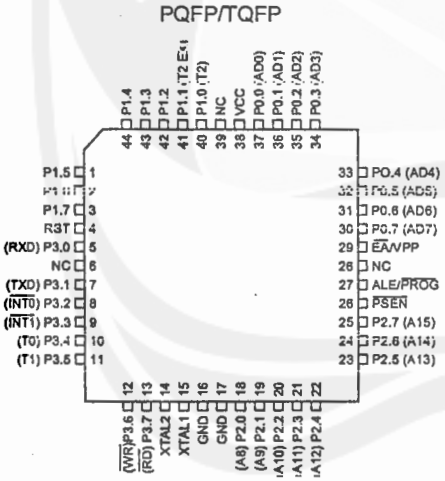
Description

The AT89C51 is a low-power, high-performance CMOS 8-bit microcomputer with 4K bytes of Flash programmable and erasable read only memory (PEROM). The device is manufactured using Atmel's high-density nonvolatile memory technology and is compatible with the industry-standard MCS-51 instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with Flash on a monolithic chip, the Atmel AT89C51 is a powerful microcomputer which provides a highly-flexible and cost-effective solution to many embedded control applications.

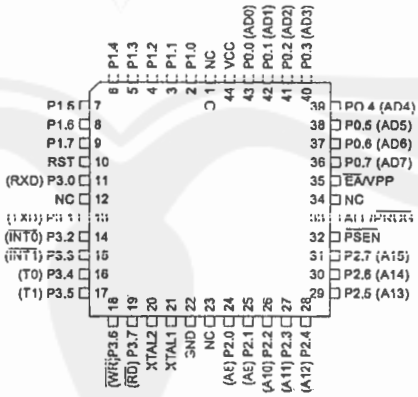
Pin Configurations

PDIP

PQFP/TQFP



PLCC



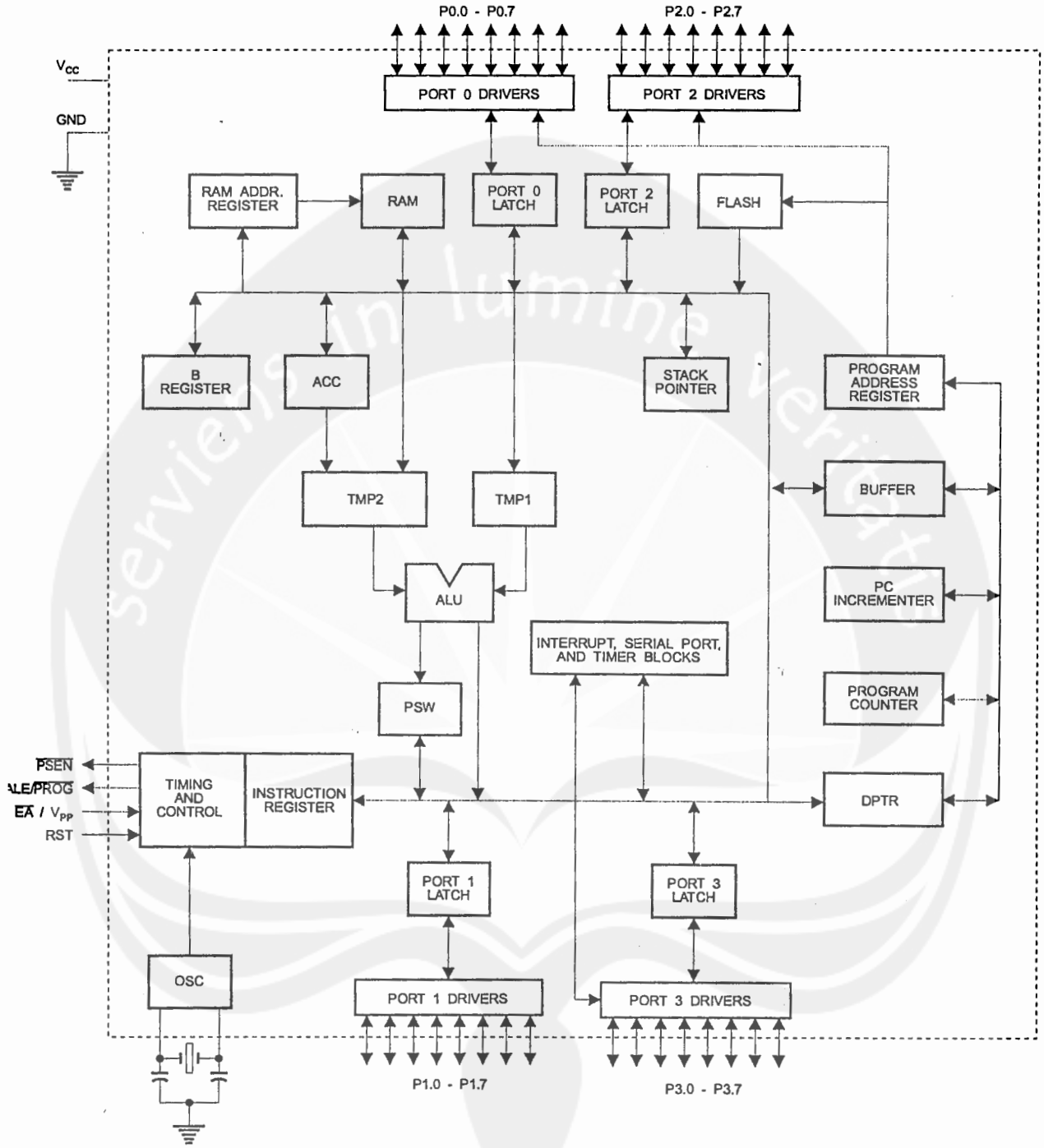
8-bit Microcontroller with 4K Bytes Flash

AT89C51

Not Recommended for New Designs. Use AT89S51.

Rev. 0200G–02/00

Block Diagram



The AT89C51 provides the following standard features: 4K bytes of Flash, 128 bytes of RAM, 32 I/O lines, two 16-bit timer/counters, a five vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator and clock circuitry. In addition, the AT89C51 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port and interrupt system to continue functioning. The Power-down Mode saves the RAM contents but freezes the oscillator disabling all other chip functions until the next hardware reset.

Pin Description

VCC

Supply voltage.

GND

Ground.

Port 0

Port 0 is an 8-bit open-drain bi-directional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 may also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode P0 has internal pullups.

Port 0 also receives the code bytes during Flash programming, and outputs the code bytes during program verification. External pullups are required during program verification.

Port 1

Port 1 is an 8-bit bi-directional I/O port with internal pullups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

Port 1 also receives the low-order address bytes during Flash programming and verification.

Port 2

Port 2 is an 8-bit bi-directional I/O port with internal pullups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, it uses strong internal pullups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3

Port 3 is an 8-bit bi-directional I/O port with internal pullups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pullups.

Port 3 also serves the functions of various special features of the AT89C51 as listed below:

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

Port 3 also receives some control signals for Flash programming and verification.

RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/$\overline{PROG}$

Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE

pulse is skipped during each access to external Data Memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

$\overline{PSEN}$

Program Store Enable is the read strobe to external program memory.

When the AT89C51 is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory.

$\overline{EA}$/VPP

External Access Enable. $\overline{EA}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming, for parts that require 12-volt V_{PP}.

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2

Output from the inverting oscillator amplifier.

Oscillator Characteristics

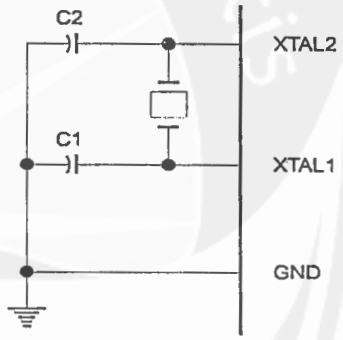
XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 1. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven as shown in Figure 2. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

It should be noted that when idle is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

Figure 1. Oscillator Connections

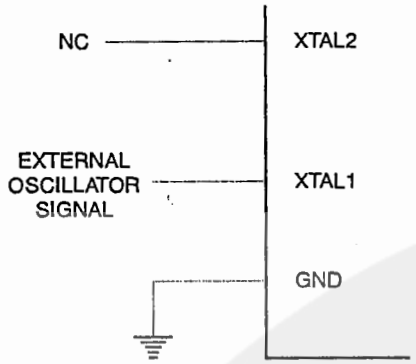


Note: C1, C2 = 30 pF ±10 pF for Crystals
= 40 pF ±10 pF for Ceramic Resonators

Status of External Pins During Idle and Power-down Modes

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

Figure 2. External Clock Drive Configuration



Power-down Mode

In the power-down mode, the oscillator is stopped, and the instruction that invokes power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the power-down mode is terminated. The only exit from power-down is a hardware reset. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Program Memory Lock Bits

On the chip are three lock bits which can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the table below.

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value, and holds that value until reset is activated. It is necessary that the latched value of $\overline{EA}$ be in agreement with the current logic level at that pin in order for the device to function properly.

Lock Bit Protection Modes

	Program Lock Bits			
	LB1	LB2	LB3	Protection Type
1	U	U	U	No program lock features
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash is disabled
3	P	P	U	Same as mode 2, also verify is disabled
4	P	P	P	Same as mode 3, also external execution is disabled

Programming the Flash

The AT89C51 is normally shipped with the on-chip Flash memory array in the erased state (that is, contents = FFH) and ready to be programmed. The programming interface accepts either a high-voltage (12-volt) or a low-voltage (V_{CC}) program enable signal. The low-voltage programming mode provides a convenient way to program the AT89C51 inside the user's system, while the high-voltage programming mode is compatible with conventional third-party Flash or EPROM programmers.

The AT89C51 is shipped with either the high-voltage or low-voltage programming mode enabled. The respective top-side marking and device signature codes are listed in the following table.

	V_{PP} = 12V	V_{PP} = 5V
Top-side Mark	AT89C51 xxxx yyww	AT89C51 xxxx-5 yyww
Signature	(030H) = 1EH (031H) = 51H (032H) =F FH	(030H) = 1EH (031H) = 51H (032H) = 05H

The AT89C51 code memory array is programmed byte-by-byte in either programming mode. *To program any non-blank byte in the on-chip Flash Memory, the entire memory must be erased using the Chip Erase Mode.*

Programming Algorithm: Before programming the AT89C51, the address, data and control signals should be set up according to the Flash programming mode table and Figure 3 and Figure 4. To program the AT89C51, take the following steps.

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ to 12V for the high-voltage programming mode.
5. Pulse ALE/$\overline{PROG}$ once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 1.5 ms. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

$\overline{Data}$ Polling: The AT89C51 features $\overline{Data}$ Polling to indicate the end of a write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written datum on PO.7. Once the write cycle has been completed, true data are valid on all outputs, and the next cycle may begin. $\overline{Data}$ Polling may begin any time after a write cycle has been initiated.

Ready/$\overline{Busy}$: The progress of byte programming can also be monitored by the RDY/$\overline{BSY}$ output signal. P3.4 is pulled low after ALE goes high during programming to indicate BUSY. P3.4 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The lock bits cannot be verified directly. Verification of the lock bits is achieved by observing that their features are enabled.

Chip Erase: The entire Flash array is erased electrically by using the proper combination of control signals and by holding ALE/$\overline{PROG}$ low for 10 ms. The code array is written with all "1"s. The chip erase operation must be executed before the code memory can be re-programmed.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 030H, 031H, and 032H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

(030H) = 1EH indicates manufactured by Atmel
(031H) = 51H indicates 89C51
(032H) = FFH indicates 12V programming
(032H) = 05H indicates 5V programming

Programming Interface

Every code byte in the Flash array can be written and the entire array can be erased by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Flash Programming Modes

Mode		RST	PSEN	ALE/PROG	EA/V_{PP}	P2.6	P2.7	P3.6	P3.7
Write Code Data		H	L		H/12V	L	H	H	H
Read Code Data		H	L	H	H	L	L	H	H
Write Lock	Bit - 1	H	L		H/12V	H	H	H	H
	Bit - 2	H	L		H/12V	H	H	L	L
	Bit - 3	H	L		H/12V	H	L	H	L
Chip Erase		H	L	(1)	H/12V	H	L	L	L
Read Signature Byte		H	L	H	H	L	L	L	L

Note: 1. Chip Erase requires a 10 ms PROG pulse.

Figure 3. Programming the Flash

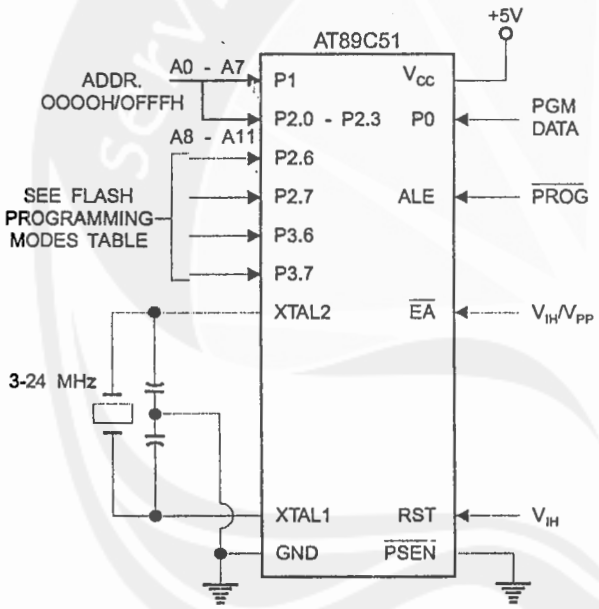
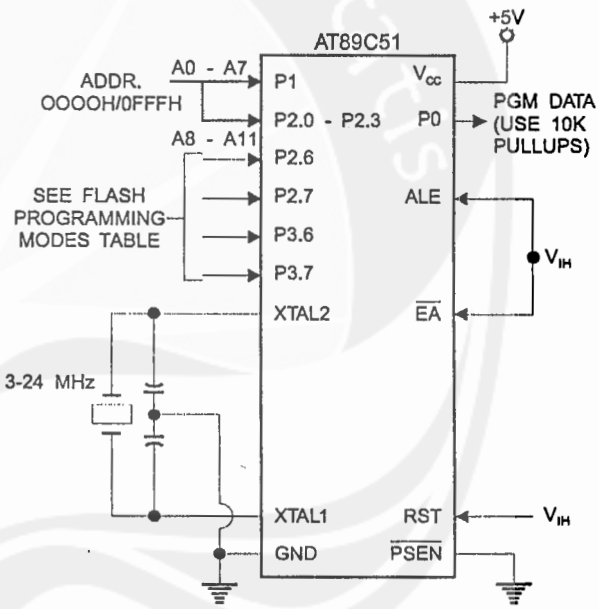
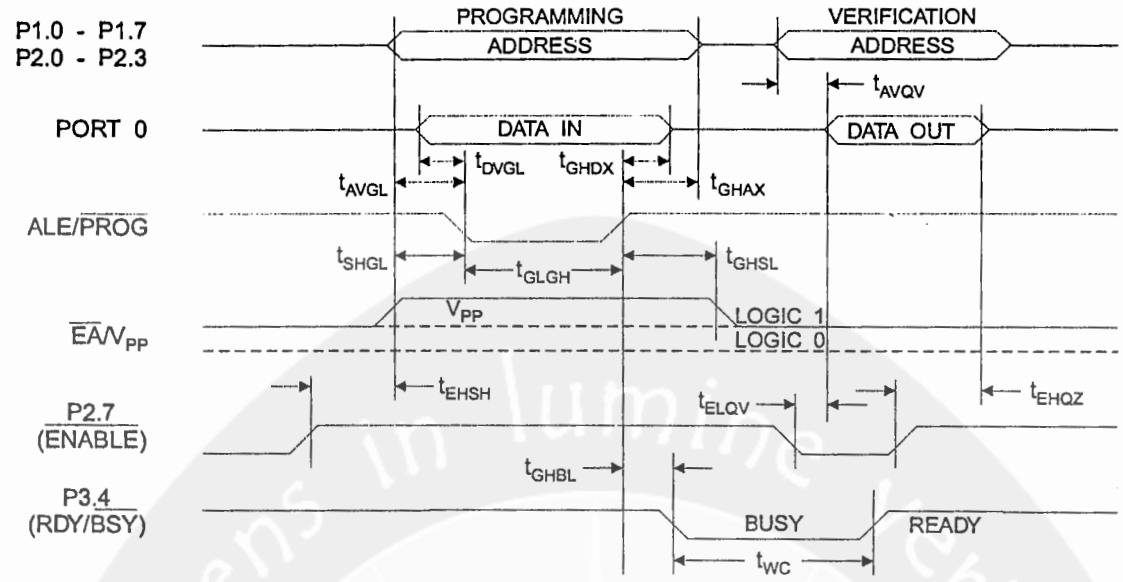


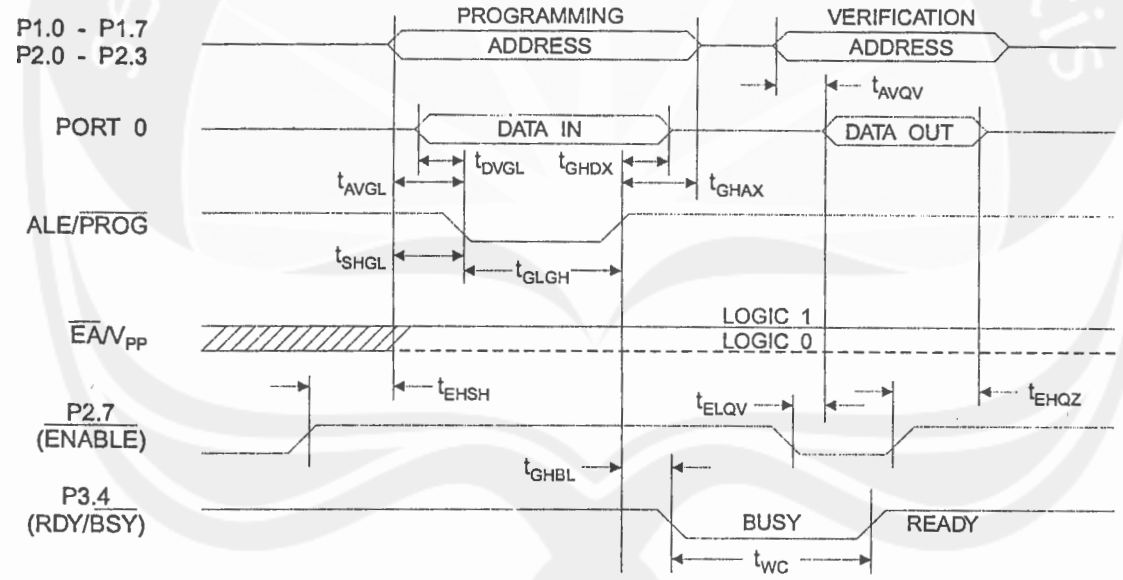
Figure 4. Verifying the Flash



Flash Programming and Verification Waveforms - High-voltage Mode (V_{PP} = 12V)



Flash Programming and Verification Waveforms - Low-voltage Mode (V_{PP} = 5V)



Flash Programming and Verification Characteristics

T_A = 0°C to 70°C, V_{CC} = 5.0 +10%

Symbol	Parameter	Min	Max	Units
V_{PP}[1]	Programming Enable Voltage	11.5	12.5	V
I_{PP}[1]	Programming Enable Current		1.0	mA
$1/t_{CLCL}$	Oscillator Frequency	3	24	MHz
t_{AVGL}	Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{GHAX}	Address Hold after $\overline{PROG}$	$48t_{CLCL}$		
t_{DVGL}	Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{GHDX}	Data Hold after $\overline{PROG}$	$48t_{CLCL}$		
t_{EHSH}	P2.7 ($\overline{ENABLE}$) High to V_{PP}	$48t_{CLCL}$		
t_{SHGL}	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
t_{GHSL}[1]	V_{PP} Hold after $\overline{PROG}$	10		µs
t_{GLGH}	$\overline{PROG}$ Width	1	110	µs
t_{AVQV}	Address to Data Valid		$48t_{CLCL}$	
t_{ELQV}	$\overline{ENABLE}$ Low to Data Valid		$48t_{CLCL}$	
t_{EHQZ}	Data Float after $\overline{ENABLE}$	0	$48t_{CLCL}$	
t_{GHBL}	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
t_{WC}	Byte Write Cycle Time		2.0	ms

Note: 1. Only used in 12-volt programming mode.

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.6V
DC Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = -40°C to 85°C, V_{CC} = 5.0V ±20% (unless otherwise noted)

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low-voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC} - 0.1	V
V_{IL1}	Input Low-voltage ($\overline{EA}$)		-0.5	0.2 V_{CC} - 0.3	V
V_{IH}	Input High-voltage	(Except XTAL1, RST)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V
V_{IH1}	Input High-voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low-voltage[1] (Ports 1,2,3)	I_{OL} = 1.6 mA		0.45	V
V_{OL1}	Output Low-voltage[1] (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.45	V
V_{OH}	Output High-voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ±10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
V_{OH1}	Output High-voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ±10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
I_{IL}	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, VCC = 5V ±10%		-650	µA
I_{LI}	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
RRST	Reset Pull-down Resistor		50	300	KΩ
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{CC}	Power Supply Current	Active Mode, 12 MHz		20	mA
		Idle Mode, 12 MHz		5	mA
	Power-down Mode[2]	V_{CC} = 6V		100	µA
		V_{CC} = 3V		40	µA

Notes:
1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum I_{OL} per 8-bit port: Port 0: 26 mA
   Ports 1, 2, 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power-down is 2V.

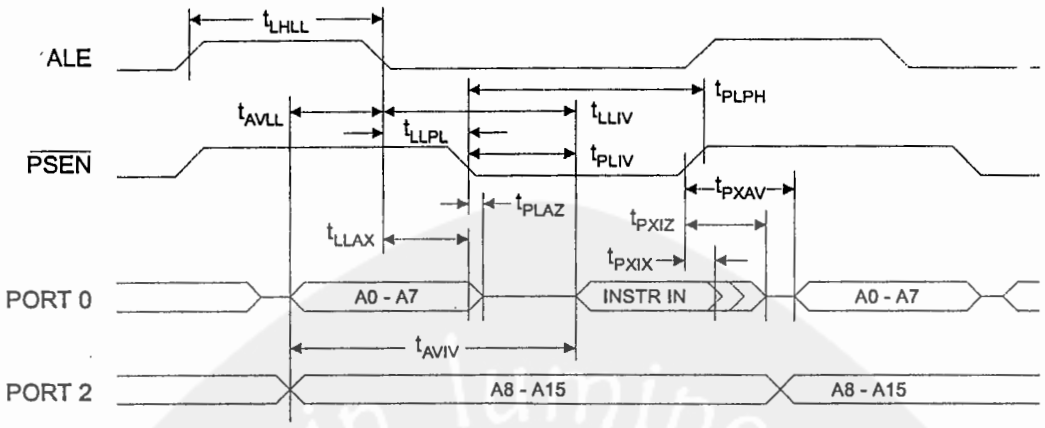
AC Characteristics

Under operating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; load capacitance for all other outputs = 80 pF.

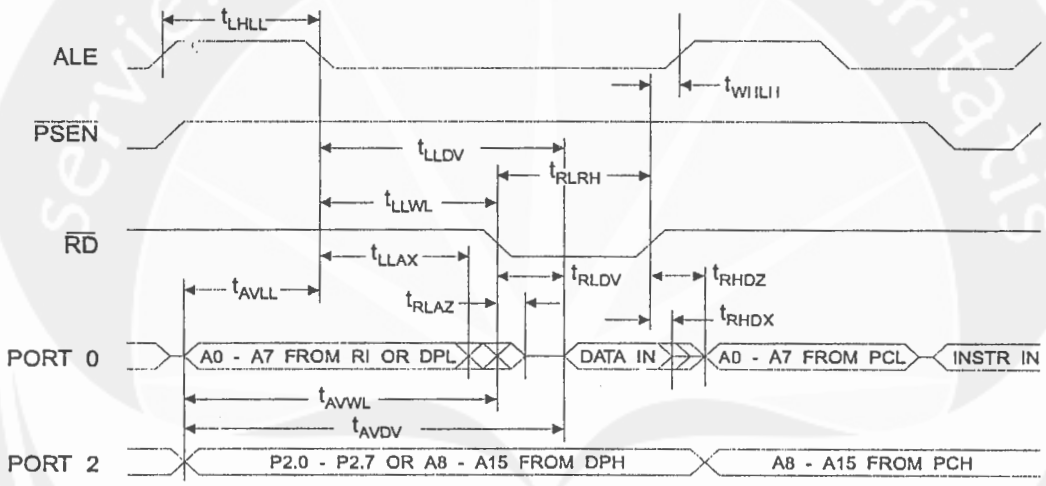
External Program and Data Memory Characteristics

Symbol	Parameter	12 MHz Oscillator		16 to 24 MHz Oscillator		Units
		Min	Max	Min	Max	
$1/t_{CLCL}$	Oscillator Frequency			0	24	MHz
t_{LHLL}	ALE Pulse Width	127		$2t_{CLCL}$ 40		ns
t_{AVLL}	Address Valid to ALE Low	43		t_{CLCL} 13		ns
t_{LLAX}	Address Hold after ALE Low	48		t_{CLCL}-20		ns
t_{LLIV}	ALE Low to Valid Instruction In		233		$4t_{CLCL}$-65	ns
t_{LLPL}	ALE Low to $\overline{PSEN}$ Low	43		t_{CLCL}-13		ns
t_{PLPH}	$\overline{PSEN}$ Pulse Width	205		$3t_{CLCL}$-20		ns
t_{PLIV}	$\overline{PSEN}$ Low to Valid Instruction In		145		$3t_{CLCL}$-45	ns
t_{PXIX}	Input Instruction Hold after $\overline{PSEN}$	0		0		ns
t_{PXIZ}	Input Instruction Float after $\overline{PSEN}$		59		t_{CLCL}-10	ns
t_{PXAV}	$\overline{PSEN}$ to Address Valid	75		t_{CLCL}-8		ns
t_{AVIV}	Address to Valid Instruction In		312		$5t_{CLCL}$-55	ns
t_{PLAZ}	$\overline{PSEN}$ Low to Address Float		10		10	ns
t_{RLRH}	$\overline{RD}$ Pulse Width	400		$6t_{CLCL}$-100		ns
t_{WLWH}	$\overline{WR}$ Pulse Width	400		$6t_{CLCL}$-100		ns
t_{RLDV}	$\overline{RD}$ Low to Valid Data In		252		$5t_{CLCL}$-90	ns
t_{RHDX}	Data Hold after $\overline{RD}$	0		0		ns
t_{RHDZ}	Data Float after $\overline{RD}$		97		$2t_{CLCL}$-28	ns
t_{LLDV}	ALE Low to Valid Data In		517		$8t_{CLCL}$-150	ns
t_{AVDV}	Address to Valid Data In		585		$9t_{CLCL}$-165	ns
t_{LLWL}	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
t_{AVWL}	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		$4t_{CLCL}$-75		ns
t_{QVWX}	Data Valid to $\overline{WR}$ Transition	23		t_{CLCL}-20		ns
t_{QVWH}	Data Valid to WR High	433		$7t_{CLCL}$-120		ns
t_{WHQX}	Data Hold after $\overline{WR}$	33		t_{CLCL}-20		ns
t_{RLAZ}	$\overline{RD}$ Low to Address Float		0		0	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	t_{CLCL}-20	t_{CLCL}+25	ns

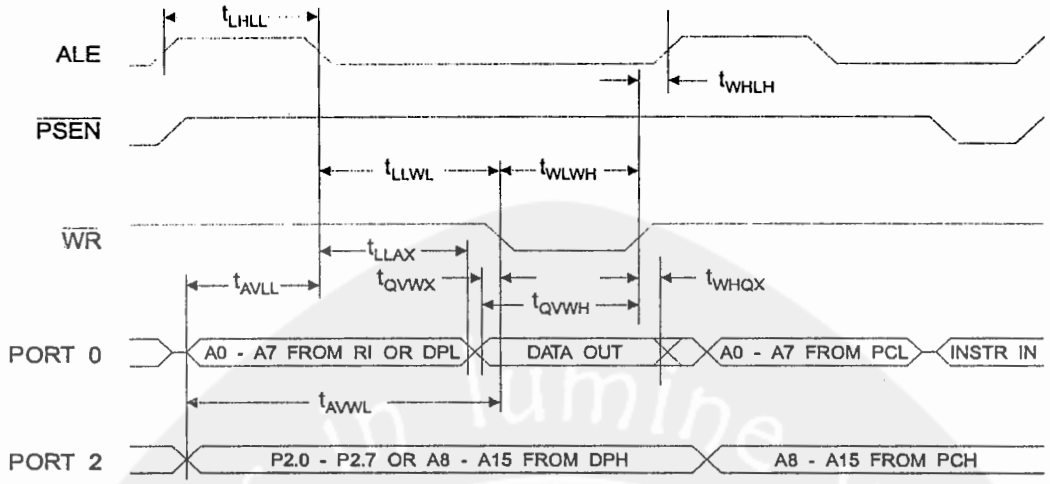
External Program Memory Read Cycle



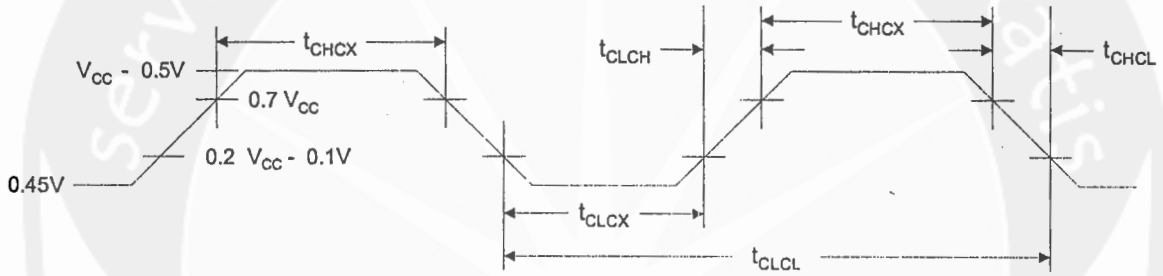
External Data Memory Read Cycle



External Data Memory Write Cycle



External Clock Drive Waveforms



External Clock Drive

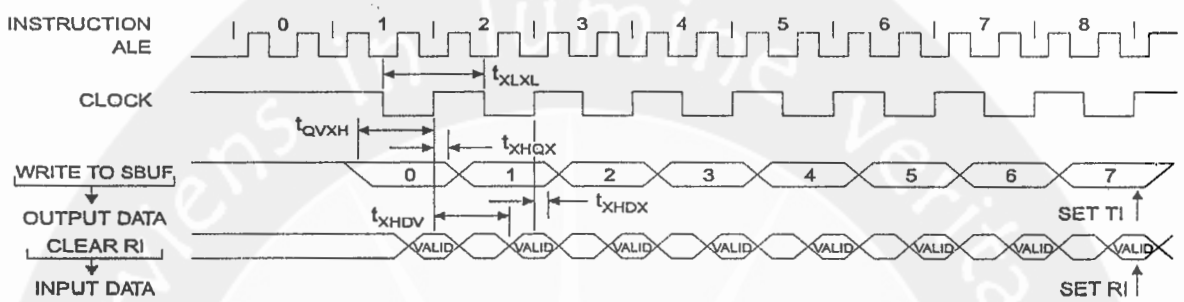
Symbol	Parameter	Min	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	0	24	MHz
t_{CLCL}	Clock Period	41.6		ns
t_{CHCX}	High Time	15		ns
t_{CLCX}	Low Time	15		ns
t_{CLCH}	Rise Time		20	ns
t_{CHCL}	Fall Time		20	ns

Serial Port Timing: Shift Register Mode Test Conditions

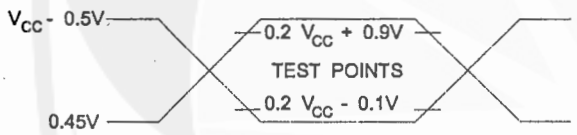
(V_{CC} = 5.0 V +20%; Load Capacitance = 80 pF)

Symbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
t_{XLXL}	Serial Port Clock Cycle Time	1.0		$12t_{CLCL}$		µs
t_{QVXH}	Output Data Setup to Clock Rising Edge	700		$10t_{CLCL}$-133		ns
t_{XHQX}	Output Data Hold after Clock Rising Edge	50		$2t_{CLCL}$-117		ns
t_{XHDX}	Input Data Hold after Clock Rising Edge	0		0		ns
t_{XHDV}	Clock Rising Edge to Input Data Valid		700		$10t_{CLCL}$-133	ns

Shift Register Mode Timing Waveforms

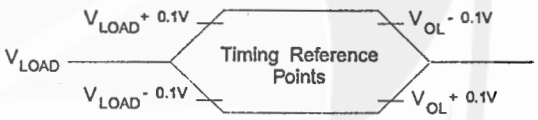


AC Testing Input/Output Waveforms[1]



Note: 1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

Float Waveforms[1]



Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

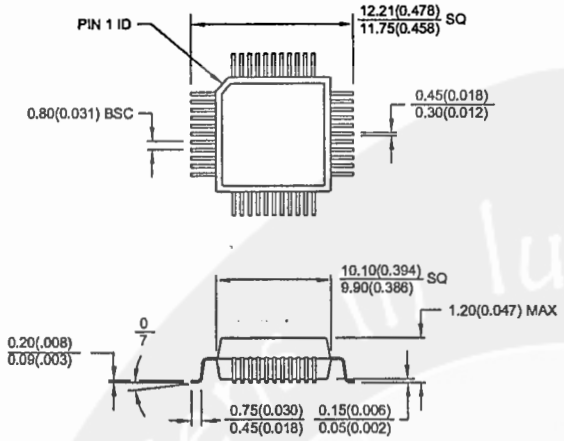
Ordering Information

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
12	5V ±20%	AT89C51-12AC	44A	Commercial
		AT89C51-12JC	44J	(0° C to 70° C)
		AT89C51-12PC	40P6	
		AT89C51-12QC	44Q	
		AT89C51-12AI	44A	Industrial
		AT89C51-12JI	44J	(-40° C to 85° C)
		AT89C51-12PI	40P6	
		AT89C51-12QI	44Q	
16	5V ±20%	AT89C51-16AC	44A	Commercial
		AT89C51-16JC	44J	(0° C to 70° C)
		AT89C51-16PC	40P6	
		AT89C51-16QC	44Q	
		AT89C51-16AI	44A	Industrial
		AT89C51-16JI	44J	(-40° C to 85° C)
		AT89C51-16PI	40P6	
		AT89C51-16QI	44Q	
20	5V ±20%	AT89C51-20AC	44A	Commercial
		AT89C51-20JC	44J	(0° C to 70° C)
		AT89C51-20PC	40P6	
		AT89C51-20QC	44Q	
		AT89C51-20AI	44A	Industrial
		AT89C51-20JI	44J	(-40° C to 85° C)
		AT89C51-20PI	40P6	
		AT89C51-20QI	44Q	
24	5V ±20%	AT89C51-24AC	44A	Commercial
		AT89C51-24JC	44J	(0° C to 70° C)
		AT89C51-24PC	40P6	
		AT89C51-24QC	44Q	
		AT89C51-24AI	44A	Industrial
		AT89C51-24JI	44J	(-40° C to 85° C)
		AT89C51-24PI	40P6	
		AT89C51-24QI	44Q	

Package Type	
44A	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
44J	44-lead, Plastic J-leaded Chip Carrier (PLCC)
40P6	40-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
44Q	44-lead, Plastic Gull Wing Quad Flatpack (PQFP)

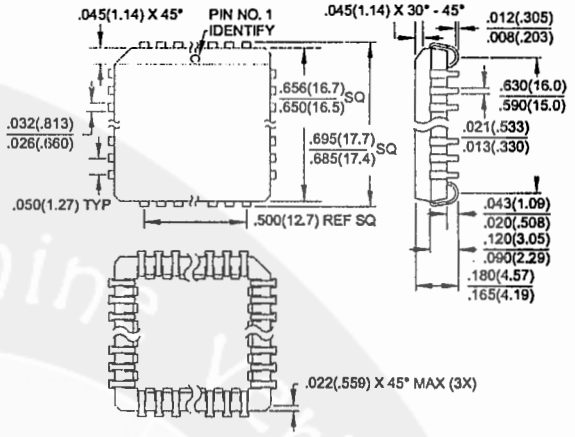
Packaging Information

44A, 44-lead, Thin (1.0 mm) Plastic Gull Wing Quad Flatpack (TQFP)
Dimensions in Millimeters and (Inches)*
JEDEC STANDARD MS-026 ACB

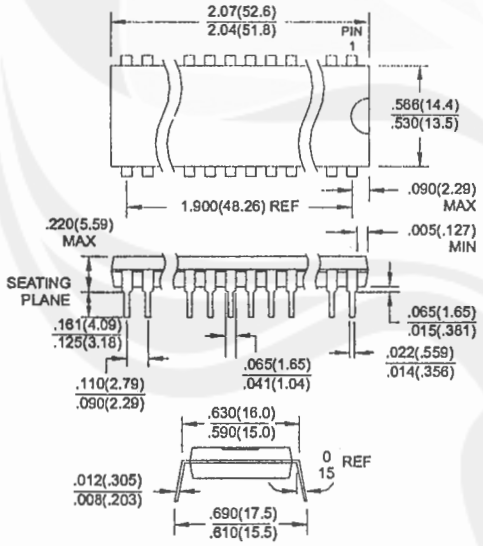


Controlling dimension: millimeters

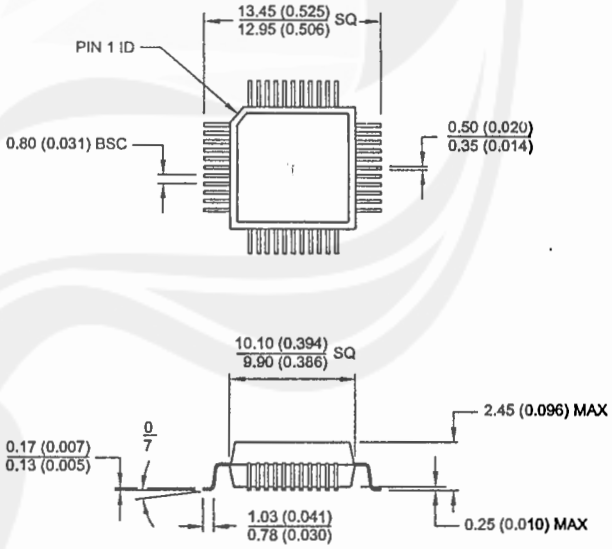
44J, 44-lead, Plastic J-leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-018 AC



40P6, 40-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)



44Q, 44-lead, Plastic Quad Flat Package (PQFP)
Dimensions in Millimeters and (Inches)*
JEDEC STANDARD MS-022 AB



Controlling dimension: millimeters

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LAMPIRAN 2

PROGRAMMER BOARD AT89C51

Using a Personal Computer to Program the AT89C51/C52/LV51/LV52/C1051/C2051

8-Bit Microcontroller with Flash

Application Note

Introduction

This application note describes a personal computer-based programmer for the AT89C51/C52/LV51/LV52/C1051/C2051 Flash-based Microcontrollers. The programmer supports all flash memory microcontroller functions, including code read, code write, chip erase, signature read, and lock bit write. When used with the AT89C51/C52/ LV51/LV52, code write, chip erase, and lock bit write may be performed at either five or twelve volts, as required by the device.

Devices sporting a "-5" suffix are intended for operation at five volts, while devices lacking the suffix operate at the standard twelve volts.

The programmer connects to an IBM PC-compatible host computer through one of the host's parallel ports. Required operating voltages are produced by an integral power supply and external, wall-mounted transformer.

Software

Software for the programmer is available by downloading it from the Atmel BBS at 408-436-4309.

The programmer is controlled by software running on the host. The AT89C51/C52 and C1051/C2051 have dedicated control programs, which were written in Microsoft C. Programs dedicated to the AT89LV51/LV52 do not exist; these devices are supported by the programs for the AT89C51/C52, respectively. In the text below, all references to the AT89C51/C52 may be assumed to apply to the AT89LV51/LV52 as well.

All programmer control programs are invoked from the DOS command line by entering the program name followed by "LPT1" or "LPT2" to specify parallel port one or two, respectively. If the parallel port is not specified, the program will respond with an error message. The control programs are menu-driven, and provide the following functions:

Chip Erase

Clear code memory to all ones. The successful operation of this function is not automatically verified.

Program from File

Write the contents of the specified file into device memory. The user is prompted for the file name, which may require path and extension.

The file is expected to contain binary data; hex files are not accepted. The first byte in the file is programmed into the first location in the device. Successive bytes are programmed into successive locations until the last location in the device has been programmed or until the data in the file has been exhausted.

Programming occurs regardless of the existing contents of device memory; a blank check is not automatically performed. After programming, the contents of device memory are not automatically verified against the file data.

Each programmed location in the device receives the maximum programming time specified in the data sheet. This is done because timing is enforced by software; the programming status information provided by $\overline{\text{DATA}}$ polling and RDY/$\overline{\text{BSY}}$ is not utilized.

The control program provides no visual indication that programming is in progress. The main menu is redisplayed when programming is complete.

0285D-B–12/97

Verify against File
Compare the contents of code memory against the contents of the specified file. The user is prompted for the file name, which may require path and extension.

The file is expected to contain binary data; hex files are not accepted. The first byte in the file is compared to the first location in the device. Successive bytes are compared to successive locations until the last location in the device has been compared or until the data in the file has been exhausted.

Locations which fail to compare are displayed by address, with the expected and actual byte contents. If there are no compare failures, nothing is displayed.

Save to File
Copy the contents of device memory to the specified file. The user is prompted for the file name, which may require path and extension. The number of bytes in the resulting file is the same as the number of memory locations in the device.

Blank Check
Verify that the contents of device memory are all ones. Only pass or fail is reported; the addresses and contents of failing locations are not displayed.

Read Signature
Read and display the contents of the signature bytes. The number of signature bytes and their expected contents varies between devices. Refer to the device data sheet for additional information.

Write Lock Bit 1
Write Lock Bit 2
Write Lock Bit 3
Set the indicated lock bit. Note that the AT89C1051/C2051 contain only two lock bits, while the AT89C51/LV51 and AT89C52/LV52 contain three lock bits. The state of the lock bits cannot be verified by direct observation.

Exit
Quit the programmer control program.

System Dependency

The control programs for the AT89C51 and AT89C52 come in two flavors: host system-dependent and host system-independent. System-dependency results from the use of software timing loops to enforce required delays, the duration of which will vary between host systems running at different speeds. The code provided was tested on an 80386-based system running at 33 MHz, and may require modification for use on other systems. This method was chosen for its simplicity.

Host system-independence is achieved by using the Programmable Interval Timer embedded in the system hardware to enforce time delays independent of system speed. The timer is reconfigured when the control program is invoked and restored to its original state before the program terminates. In order to guarantee that the program is not exited before the timer configuration is restored, the CTRL-C and CTRL-BREAK keys are disabled. This means that the program cannot be aborted except by specifying the exit option at the main menu or by rebooting the system.

The timer control code is provided as an 8086 assembly language module, which is linked with the compiled control program. The granularity of the timer is 0.838 microseconds, but the minimum practical delay is system- and software-dependent. The timer code ensures that the delay produced will not be of shorter duration than requested.

The control programs provided for the AT89C1051/C2051 are system independent.

Programmer

The programmer circuitry (see Figures 1 and 2) consists of the host interface and switchable power supplies. The signal sequencing and timing required for programming is generated by the host under software control. A 40-pin ZIF socket is provided for programming the AT89C51/C52; the 20-pin ZIF socket accommodates the AT89C1051/C2051. Note that the power and ground connections and bypass capacitors required by the TTL devices are not shown on the schematic.

Power for the programmer circuitry and the AT89C51/C52/C1051/C2051 is provided by a fixed five volt supply. A second supply provides either five or twelve volts, selectable, for use during programming. The addition of a transistor to the output of the variable supply provides a third level, ground, for use when programming the AT89C1051/C2051.

The resistor values utilized in the variable power supply circuit were determined using the equations presented in the LM317 voltage regulator data sheet. Power supply ramp rates are accommodated by the host software. For 5 V-VPP programming, the devices must be ordered from the factory as an AT89CX-XX-5 (not available with the AT89C1051/2051).

The programmer is connected to the host with a 25-conductor ribbon cable. To minimize the effect on signal integrity, the length of the cable should be as short as possible, preferably not exceeding three feet.

Parallel Interface

The original parallel interface provided by IBM was probably not intended to support bidirectional data transfers. However, due to the way in which the interface was implemented, bidirectional transfers are possible. Over the years, many products have appeared which exploit this capability.

Unfortunately, many system and interface card manufacturers have not faithfully cloned the IBM design, resulting in bus contention when the peripheral attempts to drive return

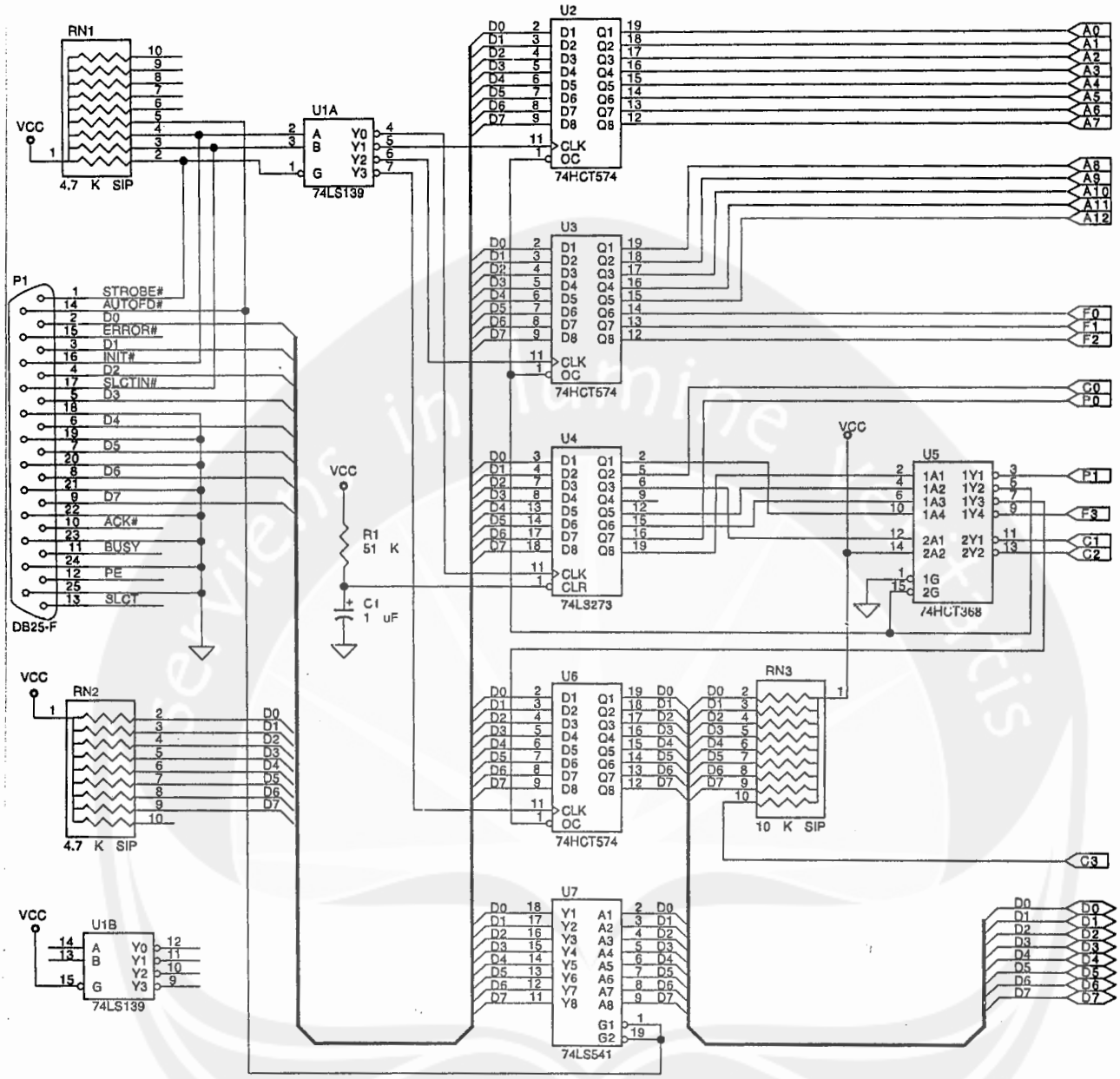
ata into the interface. Usually the peripheral drivers can verpower the interface drivers and the peripheral works, ıough this is not considered a good design practice.

lost parallel interfaces are now implemented in a single hip, such as the 82C411 or 16C452. These chips allow ıeir output drivers to be disabled under software control, roviding true bidirectional operation. The programmer oftware automatically enables bidirectional operation hen used with parallel interfaces utilizing the 82C411, 6C452, or similar chips.

ote that these chips also possess a mode control pin hich must be at the correct level to enable the directional control feature. As a result, parallel interfaces utilizing these chips cannot be assumed to be bidirectional.

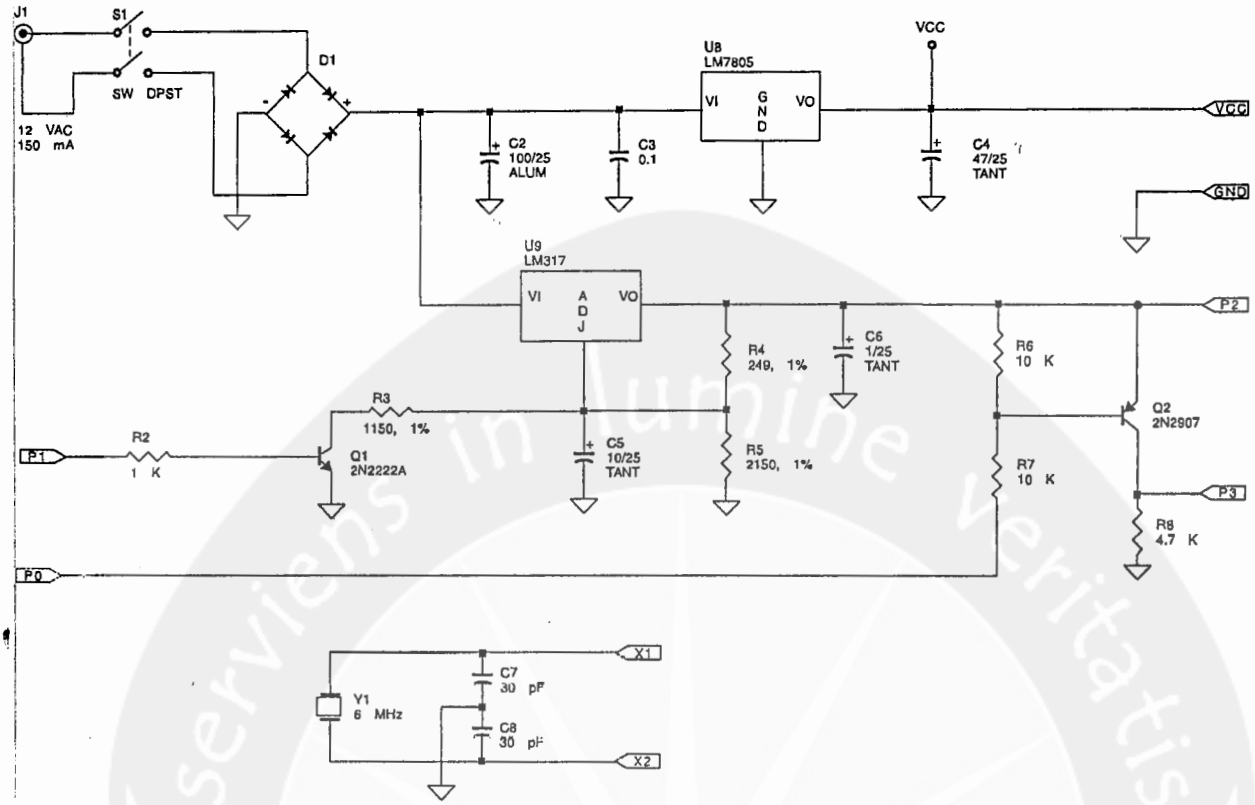
If the programmer writes devices, but fails to verify, or the signal levels at the interface don't meet TTL specifications, the parallel interface may be incompatible with the programmer. A design is provided (see Figure 4 and Figure 5) for a parallel interface which supports bidirectional operation and is compatible with the programmer. This design is simple, requiring only six ICs. The interface can be strapped to appear as LPT1 (addresses 378-37F hex) or LPT2 (278-27F hex) and will be recognized by the POST when the host system is powered up. Due to its simplicity, the parallel interface CANNOT be used as a printer interface.

Figure 1. AT89 Series Programmer Interface

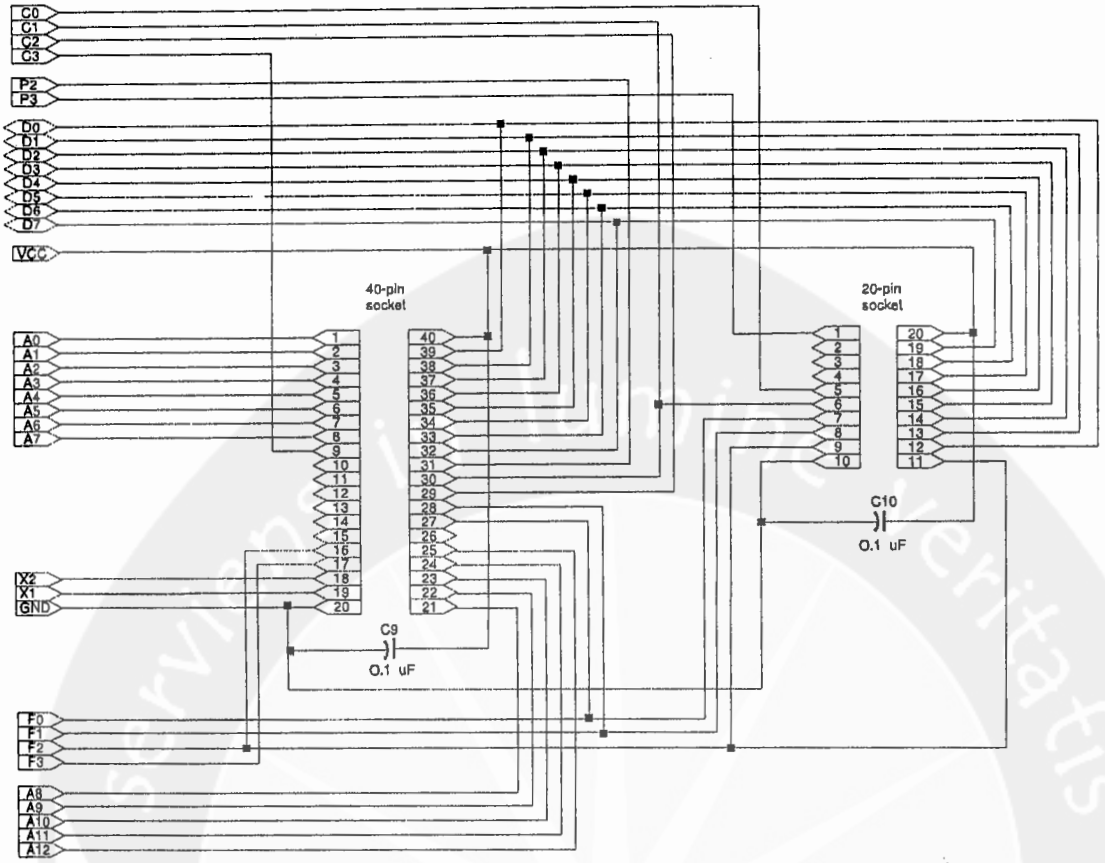


Note: 0.1 µF bypass caps on all ICs

ure 2. Power Supply for AT89 Series Programmer



ıre 3. AT89 Series Programmer Socket Wiring



ıre 4. A Parallel Interface Supporting Bidirectional Operation

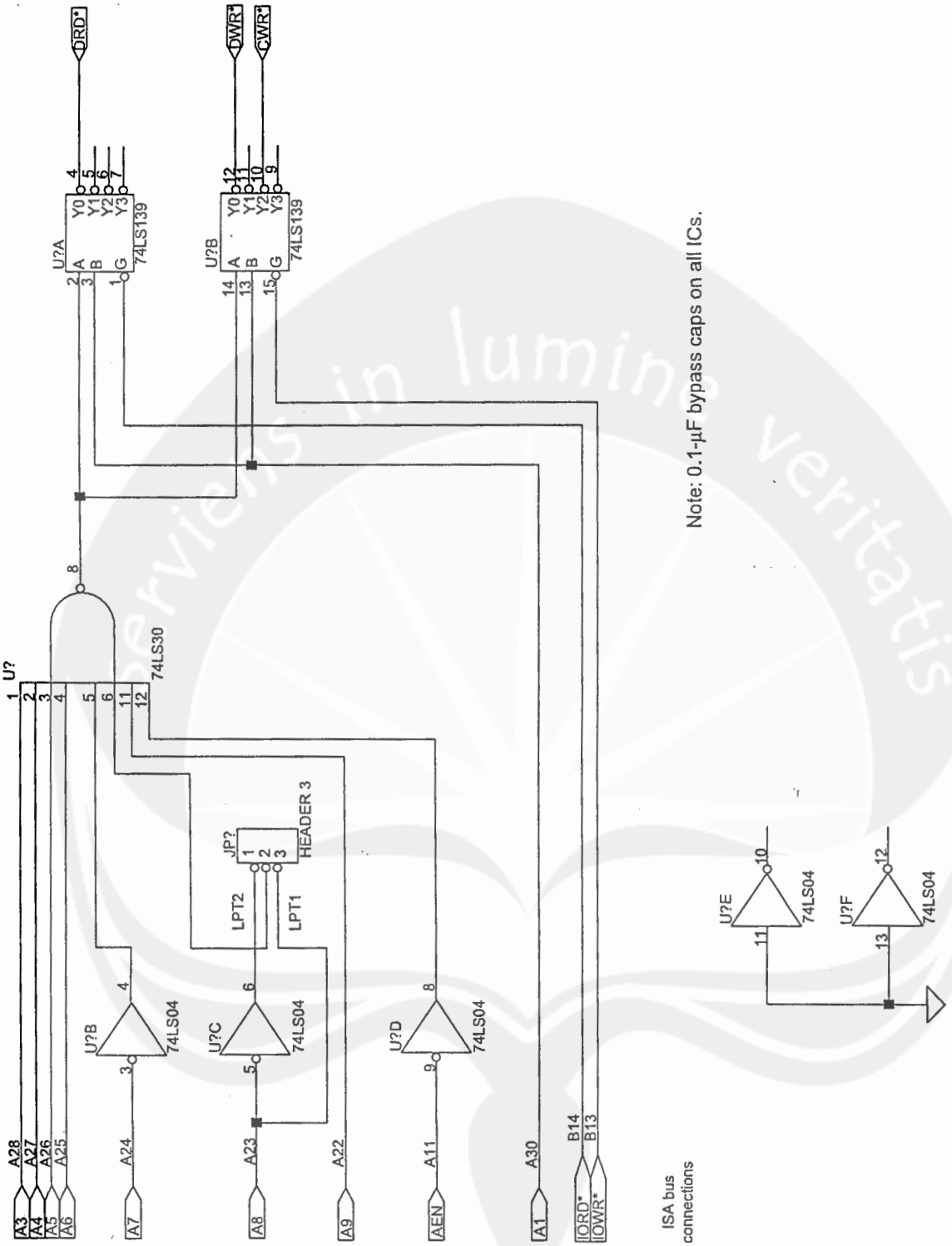
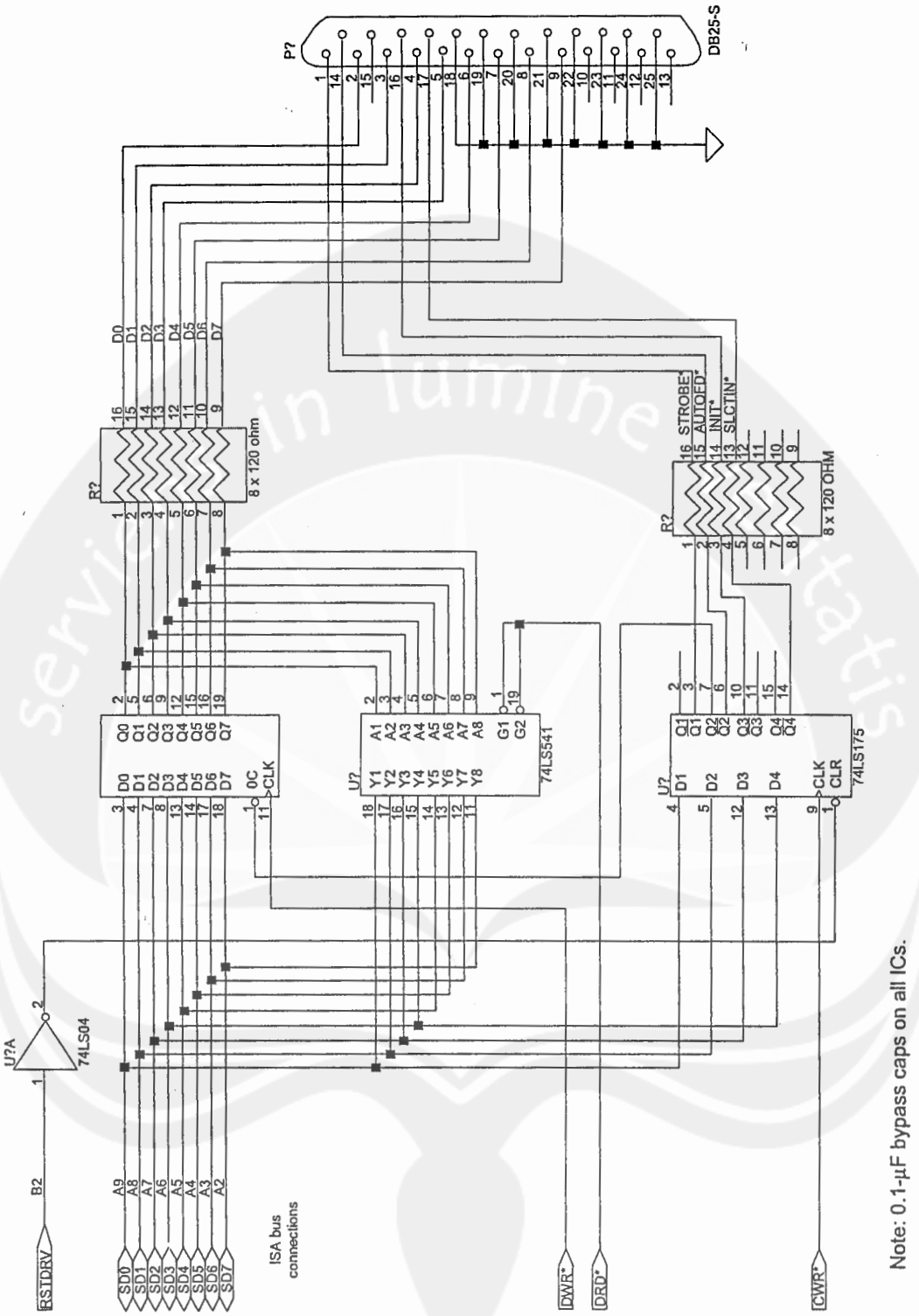


Figure 5.


P?
DB25-S
R?
8 x 120 ohm
R?
8 x 120 OHM
STROBE*
AUTOFD*
INIT*
SLCTIN*
U?
74LS541
U?
74LS175
U?A
74LS04
B2
RSTDRV
SD0
SD1
SD2
SD3
SD4
SD5
SD6
SD7
ISA bus connections
DWR*
DRD*
CWR*
Note: 0.1-µF bypass caps on all ICs.

LAMPIRAN 3

Data Sheet LM7805

MC78XX/LM78XX/MC78XXA

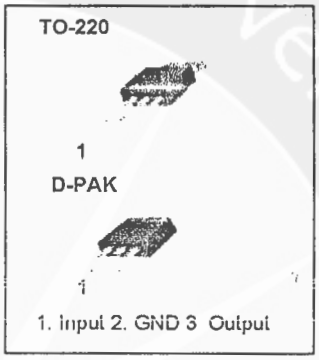
3-Terminal 1A Positive Voltage Regulator

Features

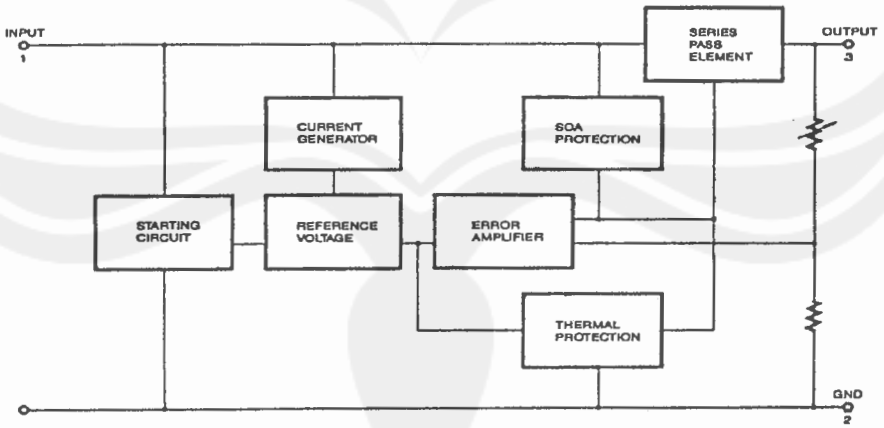
- Output Current up to 1A
- Output Voltages of 5, 6, 8, 9, 10, 12, 15, 18, 24V
- Thermal Overload Protection
- Short Circuit Protection
- Output Transistor Safe Operating Area Protection

Description

The MC78XX/LM78XX/MC78XXA series of three terminal positive regulators are available in the TO-220/D-PAK package and with several fixed output voltages, making them useful in a wide range of applications. Each type employs internal current limiting, thermal shut down and safe operating area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.



Internal Block Digram



Rev. 1.0.1

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Input Voltage (for V_O = 5V to 18V) (for V_O = 24V)	V_I V_I	35 40	V V
Thermal Resistance Junction-Cases (TO-220)	$R_{\theta JC}$	5	°C/W
Thermal Resistance Junction-Air (TO-220)	$R_{\theta JA}$	65	°C/W
Operating Temperature Range	T_{OPR}	0 ~ +125	°C
Storage Temperature Range	T_{STG}	-65 ~ +150	°C

Electrical Characteristics (MC7805/LM7805)

(Refer to test circuit ,0°C < T_J < 125°C, I_O = 500mA, V_I = 10V, C_I= 0.33µF, C_O= 0.1µF, unless otherwise specified)

Parameter	Symbol	Conditions		MC7805/LM7805 Min.	Typ.	Max.	Unit
Output Voltage	V_O	T_J =+25 °C		4.8	5.0	5.2	V
		5.0mA ≤ I_O ≤ 1.0A, P_O ≤ 15W V_I = 7V to 20V		4.75	5.0	5.25	
Line Regulation (Note1)	Regline	T_J=+25 °C	V_O = 7V to 25V	-	4.0	100	mV
			V_I = 8V to 12V	-	1.6	50	
Load Regulation (Note1)	Regload	T_J=+25 °C	I_O = 5.0mA to1.5A	-	9	100	mV
			I_O =250mA to 750mA	-	4	50	
Quiescent Current	I_Q	T_J =+25 °C		-	5.0	8.0	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1.0A		-	0.03	0.5	mA
		V_I= 7V to 25V		-	0.3	1.3	
Output Voltage Drift	$\Delta V_O/\Delta T$	I_O= 5mA		-	-0.8	-	mV/ °C
Output Noise Voltage	V_N	f = 10Hz to 100KHz, T_A=+25 °C		-	42	-	µV/Vo
Ripple Rejection	RR	f = 120Hz V_O = 8V to 18V		62	73	-	dB
Dropout Voltage	V_{Drop}	I_O = 1A, T_J =+25 °C		-	2	-	V
Output Resistance	r_O	f = 1KHz		-	15	-	mΩ
Short Circuit Current	I_{SC}	V_I = 35V, T_A =+25 °C		-	230	-	mA
Peak Current	I_{PK}	T_J =+25 °C		-	2.2	-	A

Note:

1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (MC7806)

(Refer to test circuit ,0°C < T_J < 125°C, I_O = 500mA, V_I =11V, C_I= 0.33µF, C_O= 0.1µF, unless otherwise specified)

Parameter	Symbol	Conditions		MC7806			Unit
				Min.	Typ.	Max.	
Output Voltage	V_O	T_J =+25 °C		5.75	6.0	6.25	V
		5.0mA ≤ I_O ≤ 1.0A, P_O ≤ 15W V_I = 8.0V to 21V		5.7	6.0	6.3	
Line Regulation (Note1)	Regline	T_J =+25 °C	V_I = 8V to 25V	-	5	120	mV
			V_I = 9V to 13V	-	1.5	60	
Load Regulation (Note1)	Regload	T_J =+25 °C	I_O =5mA to 1.5A	-	9	120	mV
			I_O =250mA to750A	-	3	60	
Quiescent Current	I_Q	T_J =+25 °C		-	5.0	8.0	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1A		-	-	0.5	mA
		V_I = 8V to 25V		-	-	1.3	
Output Voltage Drift	$\Delta V_O/\Delta T$	I_O = 5mA		-	-0.8	-	mV/ °C
Output Noise Voltage	V_N	f = 10Hz to 100KHz, T_A =+25 °C		-	45	-	µV/Vo
Ripple Rejection	RR	f = 120Hz V_I = 9V to 19V		59	75	-	dB
Dropout Voltage	V_{Drop}	I_O = 1A, T_J =+25 °C		-	2	-	V
Output Resistance	r_O	f = 1KHz		-	19	-	mΩ
Short Circuit Current	I_{SC}	V_I= 35V, T_A=+25 °C		-	250	-	mA
Peak Current	I_{PK}	T_J =+25 °C		-	2.2	-	A

Note:

1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (MC7808)

(Refer to test circuit ,0°C < T_J < 125°C, I_O = 500mA, V_I =14V, C_I= 0.33μF, C_O= 0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions		MC7808			Unit
				Min.	Typ.	Max.	
Output Voltage	V_O	T_J =+25 °C		7.7	8.0	8.3	V
		5.0mA ≤ I_O ≤ 1.0A, P_O ≤ 15W V_I = 10.5V to 23V		7.6	8.0	8.4	
Line Regulation (Note1)	Regline	T_J =+25 °C	V_I = 10.5V to 25V	-	5.0	160	mV
			V_I = 11.5V to 17V	-	2.0	80	
Load Regulation (Note1)	Regload	T_J =+25 °C	I_O = 5.0mA to 1.5A	-	10	160	mV
			I_O= 250mA to 750mA	-	5.0	80	
Quiescent Current	I_Q	T_J =+25 °C		-	5.0	8.0	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1.0A		-	0.05	0.5	mA
		V_I = 10.5A to 25V		-	0.5	1.0	
Output Voltage Drift	$\Delta V_O/\Delta T$	I_O = 5mA		-	-0.8	-	mV/ °C
Output Noise Voltage	V_N	f= 10Hz to 100KHz, T_A =+25 °C		-	52	-	μV/Vo
Ripple Rejection	RR	f = 120Hz, V_I= 11.5V to 21.5V		56	73	-	dB
Dropout Voltage	V_{Drop}	I_O = 1A, T_J=+25 °C		-	2	-	V
Output Resistance	r_O	f = 1KHz		-	17	-	mΩ
Short Circuit Current	I_{SC}	V_I= 35V, T_A =+25 °C		-	230	-	mA
Peak Current	I_{PK}	T_J =+25 °C		-	2.2	-	A

Note:

1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (MC7809)

(Refer to test circuit ,0°C < T_J < 125°C, I_O = 500mA, V_I =15V, C_I= 0.33µF, C_O= 0.1µF, unless otherwise specified)

Parameter	Symbol	Conditions		MC7809			Unit
				Min.	Typ.	Max.	
Output Voltage	V_O	T_J =+25°C		8.65	9	9.35	V
		5.0mA≤ I_O ≤1.0A, P_O ≤15W V_I= 11.5V to 24V		8.6	9	9.4	
Line Regulation (Note1)	Regline	T_J=+25°C	V_I = 11.5V to 25V	-	6	180	mV
			V_I = 12V to 17V	-	2	90	
Load Regulation (Note1)	Regload	T_J=+25°C	I_O = 5mA to 1.5A	-	12	180	mV
			I_O = 250mA to 750mA	-	4	90	
Quiescent Current	I_Q	T_J=+25°C		-	5.0	8.0	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1.0A		-	-	0.5	mA
		V_I = 11.5V to 26V		-	-	1.3	
Output Voltage Drift	$\Delta V_O/\Delta T$	I_O = 5mA		-	-1	-	mV/ °C
Output Noise Voltage	V_N	f = 10Hz to 100KHz, T_A =+25 °C		-	58	-	µV/Vo
Ripple Rejection	RR	f = 120Hz V_I = 13V to 23V		56	71	-	dB
Dropout Voltage	V_{Drop}	I_O = 1A, T_J=+25°C		-	2	-	V
Output Resistance	r_O	f = 1KHz		-	17	-	mΩ
Short Circuit Current	I_{SC}	V_I= 35V, T_A =+25°C		-	250	-	mA
Peak Current	I_{PK}	T_J= +25°C		-	2.2	-	A

Note:

1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (MC7812)

(Refer to test circuit ,0°C < T_J < 125°C, I_O = 500mA, V_I =19V, C_I= 0.33μF, C_O=0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions		MC7812			Unit
				Min.	Typ.	Max.	
Output Voltage	V_O	T_J =+25 °C		11.5	12	12.5	V
		5.0mA ≤ I_O≤1.0A, P_O≤15W V_I = 14.5V to 27V		11.4	12	12.6	
Line Regulation (Note1)	Regline	T_J =+25 °C	V_I = 14.5V to 30V	-	10	240	mV
			V_I = 16V to 22V	-	3.0	120	
Load Regulation (Note1)	Regload	T_J =+25 °C	I_O = 5mA to 1.5A	-	11	240	mV
			I_O = 250mA to 750mA	-	5.0	120	
Quiescent Current	I_Q	T_J =+25 °C		-	5.1	8.0	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1.0A		-	0.1	0.5	mA
		V_I = 14.5V to 30V		-	0.5	1.0	
Output Voltage Drift	$\Delta V_O/\Delta T$	I_O = 5mA		-	-1	-	mV/ °C
Output Noise Voltage	V_N	f= 10Hz to 100KHz, T_A =+25 °C		-	76	-	μV/Vo
Ripple Rejection	RR	f = 120Hz V_I = 15V to 25V		55	71	-	dB
Dropout Voltage	V_{Drop}	I_O = 1A, T_J=+25 °C		-	2	-	V
Output Resistance	r_O	f = 1KHz		-	18	-	mΩ
Short Circuit Current	I_{SC}	V_I = 35V, T_A=+25 °C		-	230	-	mA
Peak Current	I_{PK}	T_J = +25 °C		-	2.2	-	A

Note:

1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (MC7815)

(Refer to test circuit ,0°C < T_J < 125°C, I_O = 500mA, V_I =23V, C_I= 0.33µF, C_O=0.1µF, unless otherwise specified)

Parameter	Symbol	Conditions		MC7815			Unit
				Min.	Typ.	Max.	
Output Voltage	V_O	T_J =+25 °C		14.4	15	15.6	V
		5.0mA ≤ I_O ≤ 1.0A, P_O ≤ 15W V_I = 17.5V to 30V		14.25	15	15.75	
Line Regulation (Note1)	Regline	T_J =+25 °C	V_I = 17.5V to 30V	-	11	300	mV
			V_I = 20V to 26V	-	3	150	
Load Regulation (Note1)	Regload	T_J =+25 °C	I_O = 5mA to 1.5A	-	12	300	mV
			I_O = 250mA to 750mA	-	4	150	
Quiescent Current	I_Q	T_J =+25 °C		-	5.2	8.0	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1.0A		-	-	0.5	mA
		V_I = 17.5V to 30V		-	-	1.0	
Output Voltage Drift	$\Delta V_O/\Delta T$	I_O = 5mA		-	-1	-	mV/ °C
Output Noise Voltage	V_N	f = 10Hz to 100KHz, T_A =+25 °C		-	90	-	µV/Vo
Ripple Rejection	RR	f = 120Hz V_I = 18.5V to 28.5V		54	70	-	dB
Dropout Voltage	V_{Drop}	I_O = 1A, T_J=+25 °C		-	2	-	V
Output Resistance	r_O	f = 1KHz		-	19	-	mΩ
Short Circuit Current	I_{SC}	V_I = 35V, T_A=+25 °C		-	250	-	mA
Peak Current	I_{PK}	T_J =+25 °C		-	2.2	-	A

Note:

1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (MC7824)

(Refer to test circuit ,0°C < T_J < 125°C, I_O = 500mA, V_I =33V, C_I= 0.33µF, C_O=0.1µF, unless otherwise specified)

Parameter	Symbol	Conditions		MC7824			Unit
				Min.	Typ.	Max.	
Output Voltage	V_O	T_J =+25 °C		23	24	25	V
		5.0mA ≤ I_O ≤ 1.0A, P_O ≤ 15W V_I = 27V to 38V		22.8	24	25.25	
Line Regulation (Note1)	Regline	T_J =+25 °C	V_I = 27V to 38V	-	17	480	mV
			V_I = 30V to 36V	-	6	240	
Load Regulation (Note1)	Regload	T_J =+25 °C	I_O = 5mA to 1.5A	-	15	480	mV
			I_O = 250mA to 750mA	-	5.0	240	
Quiescent Current	I_Q	T_J =+25 °C		-	5.2	8.0	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1.0A		-	0.1	0.5	mA
		V_I = 27V to 38V		-	0.5	1	
Output Voltage Drift	$\Delta V_O/\Delta T$	I_O = 5mA		-	-1.5	-	mV/ °C
Output Noise Voltage	V_N	f = 10Hz to 100KHz, T_A =+25 °C		-	60	-	µV/Vo
Ripple Rejection	RR	f = 120Hz V_I = 28V to 38V		50	67	-	dB
Dropout Voltage	V_{Drop}	I_O = 1A, T_J=+25 °C		-	2	-	V
Output Resistance	r_O	f = 1KHz		-	28	-	mΩ
Short Circuit Current	I_{SC}	V_I = 35V, T_A=+25 °C		-	230	-	mA
Peak Current	I_{PK}	T_J =+25 °C		-	2.2	-	A

Note:

1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (MC7805A)

(Refer to the test circuits. 0°C < T_J < 125°C, I_O =1A, V_I = 10V, C_I=0.33μF, C_O=0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Output Voltage	V_O	T_J =+25 °C		4.9	5	5.1	V
		I_O = 5mA to 1A, P_O ≤ 15W V_I = 7.5V to 20V		4.8	5	5.2	
Line Regulation (Note1)	Regline	V_I = 7.5V to 25V I_O = 500mA		-	5	50	mV
		V_I = 8V to 12V		-	3	50	
		T_J =+25 °C	V_I= 7.3V to 20V	-	5	50	
			V_I= 8V to 12V	-	1.5	25	
Load Regulation (Note1)	Regload	T_J =+25 °C I_O = 5mA to 1.5A		-	9	100	mV
		I_O = 5mA to 1A		-	9	100	
		I_O = 250mA to 750mA		-	4	50	
Quiescent Current	I_Q	T_J =+25 °C		-	5.0	6	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1A		-	-	0.5	mA
		V_I = 8 V to 25V, I_O = 500mA		-	-	0.8	
		V_I = 7.5V to 20V, T_J =+25 °C		-	-	0.8	
Output Voltage Drift	$\Delta V/\Delta T$	Io = 5mA		-	-0.8	-	mV/ °C
Output Noise Voltage	V_N	f = 10Hz to 100KHz T_A =+25 °C		-	10	-	μV/Vo
Ripple Rejection	RR	f = 120Hz, I_O = 500mA V_I = 8V to 18V		-	68	-	dB
Dropout Voltage	V_{Drop}	I_O = 1A, T_J =+25 °C		-	2	-	V
Output Resistance	r_O	f = 1KHz		-	17	-	mΩ
Short Circuit Current	I_{SC}	V_I= 35V, T_A =+25 °C		-	250	-	mA
Peak Current	I_{PK}	T_J= +25 °C		-	2.2	-	A

Note:

1. Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (MC7806A)

(Refer to the test circuits. 0°C < T_J < 125°C, I_O =1A, V_I =11V, C_I=0.33μF, C_O=0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Output Voltage	V_O	T_J =+25 °C		5.58	6	6.12	V
		I_O = 5mA to 1A, P_O ≤ 15W V_I = 8.6V to 21V		5.76	6	6.24	
Line Regulation (Note1)	Regline	V_I= 8.6V to 25V I_O = 500mA		-	5	60	mV
		V_I= 9V to 13V		-	3	60	
		T_J =+25 °C	V_I= 8.3V to 21V	-	5	60	
			V_I= 9V to 13V	-	1.5	30	
Load Regulation (Note1)	Regload	T_J =+25 °C I_O = 5mA to 1.5A		-	9	100	mV
		I_O = 5mA to 1A		-	4	100	
		I_O = 250mA to 750mA		-	5.0	50	
Quiescent Current	I_Q	T_J =+25 °C		-	4.3	6	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1A		-	-	0.5	mA
		V_I = 9V to 25V, I_O = 500mA		-	-	0.8	
		V_I= 8.5V to 21V, T_J =+25 °C		-	-	0.8	
Output Voltage Drift	$\Delta V/\Delta T$	I_O = 5mA		-	-0.8	-	mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz T_A =+25 °C		-	10	-	μV/Vo
Ripple Rejection	RR	f = 120Hz, I_O = 500mA V_I = 9V to 19V		-	65	-	dB
Dropout Voltage	V_{Drop}	I_O = 1A, T_J =+25 °C		-	2	-	V
Output Resistance	r_O	f = 1KHz		-	17	-	mΩ
Short Circuit Current	I_{SC}	V_I= 35V, T_A =+25 °C		-	250	-	mA
Peak Current	I_{PK}	T_J=+25 °C		-	2.2	-	A

Note:

1. Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (MC7808A)

(Refer to the test circuits. 0°C < T_J < 125°C, I_O =1A, V_I = 14V, C_I=0.33μF, C_O=0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Output Voltage	V_O	T_J =+25 °C		7.84	8	8.16	V
		I_O = 5mA to 1A, P_O ≤15W V_I = 10.6V to 23V		7.7	8	8.3	
Line Regulation (Note1)	Regline	V_I= 10.6V to 25V I_O = 500mA		-	6	80	mV
		V_I= 11V to 17V		-	3	80	
		T_J =+25 °C	V_I= 10.4V to 23V	-	6	80	
			V_I= 11V to 17V	-	2	40	
Load Regulation (Note1)	Regload	T_J =+25 °C I_O = 5mA to 1.5A		-	12	100	mV
		I_O = 5mA to 1A		-	12	100	
		I_O = 250mA to 750mA		-	5	50	
Quiescent Current	I_Q	T_J =+25 °C		-	5.0	6	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1A		-	-	0.5	mA
		V_I = 11V to 25V, I_O = 500mA		-	-	0.8	
		V_I= 10.6V to 23V, T_J =+25 °C		-	-	0.8	
Output Voltage Drift	$\Delta V/\Delta T$	I_O = 5mA		-	-0.8	-	mV/ °C
Output Noise Voltage	V_N	f = 10Hz to 100KHz T_A =+25 °C		-	10	-	μV/Vo
Ripple Rejection	RR	f = 120Hz, I_O = 500mA V_I = 11.5V to 21.5V		-	62	-	dB
Dropout Voltage	V_{Drop}	I_O = 1A, T_J =+25 °C		-	2	-	V
Output Resistance	r_O	f = 1KHz		-	18	-	mΩ
Short Circuit Current	I_{SC}	V_I= 35V, T_A =+25 °C		-	250	-	mA
Peak Current	I_{PK}	T_J=+25 °C		-	2.2	-	A

Note:

1. Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (MC7809A)

(Refer to the test circuits. 0°C < T_J < 125°C, I_O =1A, V_I = 15V, C_I=0.33μF, C_O=0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Voltage	V_O	T_J =+25°C	8.82	9.0	9.18	V
		I_O = 5mA to 1A, P_O≤15W V_I = 11.2V to 24V	8.65	9.0	9.35	
Line Regulation (Note1)	Regline	V_I= 11.7V to 25V I_O = 500mA	-	6	90	mV
		V_I= 12.5V to 19V	-	4	45	
		T_J =+25°C, V_I= 11.5V to 24V	-	6	90	
		T_J =+25°C, V_I= 12.5V to 19V	-	2	45	
Load Regulation (Note1)	Regload	T_J =+25°C I_O = 5mA to 1.0A	-	12	100	mV
		I_O = 5mA to 1.0A	-	12	100	
		I_O = 250mA to 750mA	-	5	50	
Quiescent Current	I_Q	T_J =+25 °C	-	5.0	6.0	mA
Quiescent Current Change	ΔI_Q	V_I = 11.7V to 25V, T_J=+25 °C	-	-	0.8	mA
		V_I = 12V to 25V, I_O = 500mA	-	-	0.8	
		I_O = 5mA to 1.0A	-	-	0.5	
Output Voltage Drift	$\Delta V/\Delta T$	I_O = 5mA	-	-1.0	-	mV/ °C
Output Noise Voltage	V_N	f = 10Hz to 100KHz T_A =+25 °C	-	10	-	μV/Vo
Ripple Rejection	RR	f = 120Hz, I_O = 500mA V_I = 12V to 22V	-	62	-	dB
Dropout Voltage	V_{Drop}	I_O = 1A, T_J =+25 °C	-	2.0	-	V
Output Resistance	r_O	f = 1KHz	-	17	-	mΩ
Short Circuit Current	I_{SC}	V_I= 35V, T_A =+25 °C	-	250	-	mA
Peak Current	I_{PK}	T_J=+25°C	-	2.2	-	A

Note:

1. Load and line regulation are specified at constant, junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (MC7810A)

(Refer to the test circuits. 0°C < T_J < 125°C, I_O =1A, V_I = 16V, C_I=0.33μF, C_O=0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Output Voltage	V_O	T_J =+25°C		9.8	10	10.2	V
		I_O = 5mA to 1A, P_O ≤ 15W V_I =12.8V to 25V		9.6	10	10.4	
Line Regulation (Note1)	Regline	V_I= 12.8V to 26V I_O = 500mA		-	8	100	mV
		V_I= 13V to 20V		-	4	50	
		T_J =+25°C	V_I= 12.5V to 25V	-	8	100	
			V_I= 13V to 20V	-	3	50	
Load Regulation (Note1)	Regload	T_J =+25°C I_O = 5mA to 1.5A		-	12	100	mV
		I_O = 5mA to 1.0A		-	12	100	
		I_O = 250mA to 750mA		-	5	50	
Quiescent Current	I_Q	T_J =+25°C		-	5.0	6.0	mA
Quiescent Current Change	ΔI_Q	V_I = 13V to 26V, T_J=+25°C		-	-	0.5	mA
		V_I = 12.8V to 25V, I_O = 500mA		-	-	0.8	
		I_O = 5mA to 1.0A		-	-	0.5	
Output Voltage Drift	$\Delta V/\Delta T$	I_O = 5mA		-	-1.0	-	mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz T_A =+25°C		-	10	-	μV/Vo
Ripple Rejection	RR	f = 120Hz, I_O = 500mA V_I = 14V to 24V		-	62	-	dB
Dropout Voltage	V_{Drop}	I_O = 1A, T_J =+25°C		-	2.0	-	V
Output Resistance	r_O	f = 1KHz		-	17	-	mΩ
Short Circuit Current	I_{SC}	V_I= 35V, T_A =+25°C		-	250	-	mA
Peak Current	I_{PK}	T_J=+25°C		-	2.2	-	A

Note:

1. Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (MC7812A)

(Refer to the test circuits. 0°C < T_J < 125°C, I_O =1A, V_I = 19V, C_I=0.33μF, C_O=0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Output Voltage	V_O	T_J =+25 °C		11.75	12	12.25	V
		I_O = 5mA to 1A, P_O ≤15W V_I = 14.8V to 27V		11.5	12	12.5	
Line Regulation (Note1)	Regline	V_I= 14.8V to 30V I_O = 500mA		-	10	120	mV
		V_I= 16V to 22V		-	4	120	
		T_J =+25 °C	V_I= 14.5V to 27V	-	10	120	
			V_I= 16V to 22V	-	3	60	
Load Regulation (Note1)	Regload	T_J =+25 °C I_O = 5mA to 1.5A		-	12	100	mV
		I_O = 5mA to 1.0A		-	12	100	
		I_O = 250mA to 750mA		-	5	50	
Quiescent Current	I_Q	T_J =+25°C		-	5.1	6.0	mA
Quiescent Current Change	ΔI_Q	V_I = 15V to 30V, T_J=+25 °C		-		0.8	mA
		V_I = 14V to 27V, I_O = 500mA		-		0.8	
		I_O = 5mA to 1.0A		-		0.5	
Output Voltage Drift	$\Delta V/\Delta T$	I_O = 5mA		-	-1.0	-	mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz T_A =+25°C		-	10	-	μV/Vo
Ripple Rejection	RR	f = 120Hz, I_O = 500mA V_I = 14V to 24V		-	60	-	dB
Dropout Voltage	V_{Drop}	I_O = 1A, T_J =+25°C		-	2.0	-	V
Output Resistance	r_O	f = 1KHz		-	18	-	mΩ
Short Circuit Current	I_{SC}	V_I= 35V, T_A =+25 °C		-	250	-	mA
Peak Current	I_{PK}	T_J=+25 °C		-	2.2	-	A

Note:

1. Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (MC7815A)

(Refer to the test circuits. 0°C < T_J < 125°C, I_O =1A, V_I =23V, C_I=0.33μF, C_O=0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Output Voltage	V_O	T_J =+25 °C		14.7	15	15.3	V
		I_O = 5mA to 1A, P_O ≤15W V_I = 17.7V to 30V		14.4	15	15.6	
Line Regulation (Note1)	Regline	V_I= 17.9V to 30V I_O = 500mA		-	10	150	mV
		V_I= 20V to 26V		-	5	150	
		T_J =+25°C	V_I= 17.5V to 30V	-	11	150	
			V_I= 20V to 26V	-	3	75	
Load Regulation (Note1)	Regload	T_J =+25 °C I_O = 5mA to 1.5A		-	12	100	mV
		I_O = 5mA to 1.0A		-	12	100	
		I_O = 250mA to 750mA		-	5	50	
Quiescent Current	I_Q	T_J =+25 °C		-	5.2	6.0	mA
Quiescent Current Change	ΔI_Q	V_I = 17.5V to 30V, T_J =+25 °C		-	-	0.8	mA
		V_I = 17.5V to 30V, I_O = 500mA		-	-	0.8	
		I_O = 5mA to 1.0A		-	-	0.5	
Output Voltage Drift	$\Delta V/\Delta T$	I_O = 5mA		-	-1.0	-	mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz T_A =+25 °C		-	10	-	μV/Vo
Ripple Rejection	RR	f = 120Hz, I_O = 500mA V_I = 18.5V to 28.5V		-	58	-	dB
Dropout Voltage	V_{Drop}	I_O = 1A, T_J =+25 °C		-	2.0	-	V
Output Resistance	r_O	f = 1KHz		-	19	-	mΩ
Short Circuit Current	I_{SC}	V_I= 35V, T_A =+25 °C		-	250	-	mA
Peak Current	I_{PK}	T_J=+25°C		-	2.2	-	A

Note:

1. Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (MC7818A)

(Refer to the test circuits. 0°C < T_J < 125°C, I_O =1A, V_I = 27V, C_I=0.33μF, C_O=0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Output Voltage	V_O	T_J =+25 °C		17.64	18	18.36	V
		I_O = 5mA to 1A, P_O ≤15W V_I = 21V to 33V		17.3	18	18.7	
Line Regulation (Note1)	Regline	V_I= 21V to 33V I_O = 500mA		-	15	180	mV
		V_I= 21V to 33V		-	5	180	
		T_J =+25 °C	V_I= 20.6V to 33V	-	15	180	
			V_I= 24V to 30V	-	5	90	
Load Regulation (Note1)	Regload	T_J =+25°C I_O = 5mA to 1.5A		-	15	100	mV
		I_O = 5mA to 1.0A		-	15	100	
		I_O = 250mA to 750mA		-	7	50	
Quiescent Current	I_Q	T_J =+25 °C		-	5.2	6.0	mA
Quiescent Current Change	ΔI_Q	V_I = 21V to 33V, T_J=+25 °C		-	-	0.8	mA
		V_I = 21V to 33V, I_O = 500mA		-	-	0.8	
		I_O = 5mA to 1.0A		-	-	0.5	
Output Voltage Drift	$\Delta V/\Delta T$	I_O = 5mA		-	-1.0	-	mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz T_A =+25°C		-	10	-	μV/Vo
Ripple Rejection	RR	f = 120Hz, I_O = 500mA V_I = 22V to 32V		-	57	-	dB
Dropout Voltage	V_{Drop}	I_O = 1A, T_J =+25°C		-	2.0	-	V
Output Resistance	r_O	f = 1KHz		-	19	-	mΩ
Short Circuit Current	I_{SC}	V_I= 35V, T_A =+25°C		-	250	-	mA
Peak Current	I_{PK}	T_J=+25 °C		-	2.2	-	A

Note:

1. Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (MC7824A)

(Refer to the test circuits. 0°C < T_J < 125°C, I_O =1A, V_I = 33V, C_I=0.33μF, C_O=0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Output Voltage	V_O	T_J =+25 °C		23.5	24	24.5	V
		I_O = 5mA to 1A, P_O ≤15W V_I = 27.3V to 38V		23	24	25	
Line Regulation (Note1)	Regline	V_I= 27V to 38V I_O = 500mA		-	18	240	mV
		V_I= 21V to 33V		-	6	240	
		T_J =+25 °C	V_I= 26.7V to 38V	-	18	240	
			V_I= 30V to 36V	-	6	120	
Load Regulation (Note1)	Regload	T_J =+25 °C I_O = 5mA to 1.5A		-	15	100	mV
		I_O = 5mA to 1.0A		-	15	100	
		I_O = 250mA to 750mA		-	7	50	
Quiescent Current	I_Q	T_J =+25 °C		-	5.2	6.0	mA
Quiescent Current Change	ΔI_Q	V_I = 27.3V to 38V, T_J =+25 °C		-	-	0.8	mA
		V_I = 27.3V to 38V, I_O = 500mA		-	-	0.8	
		I_O = 5mA to 1.0A		-	-	0.5	
Output Voltage Drift	$\Delta V/\Delta T$	I_O = 5mA		-	-1.5	-	mV/ °C
Output Noise Voltage	V_N	f = 10Hz to 100KHz T_A = 25 °C		-	10	-	μV/Vo
Ripple Rejection	RR	f = 120Hz, I_O = 500mA V_I = 28V to 38V		-	54	-	dB
Dropout Voltage	V_{Drop}	I_O = 1A, T_J =+25 °C		-	2.0	-	V
Output Resistance	r_O	f = 1KHz		-	20	-	mΩ
Short Circuit Current	I_{SC}	V_I= 35V, T_A =+25 °C		-	250	-	mA
Peak Current	I_{PK}	T_J=+25 °C		-	2.2	-	A

Note:

1. Load and line regulation are specified at constant junction temperature. Change in VO due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Typical Perfomance Characteristics

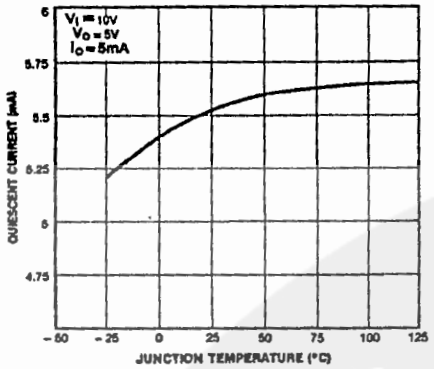


Figure 1. Quiescent Current

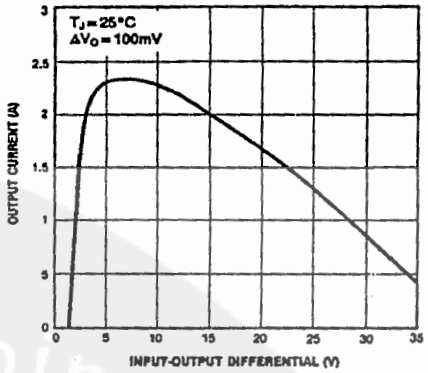


Figure 2. Peak Output Current

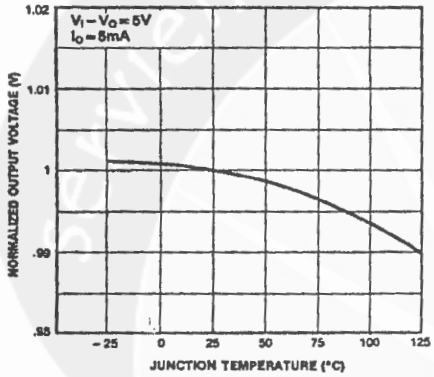


Figure 3. Output Voltage

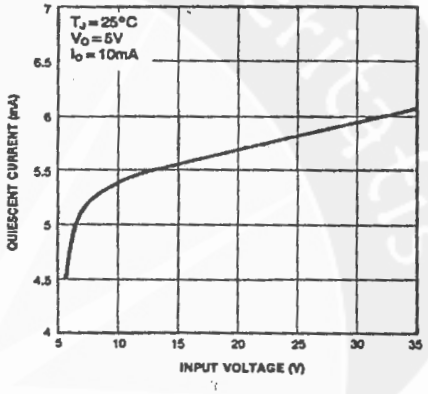


Figure 4. Quiescent Current

Typical Applications

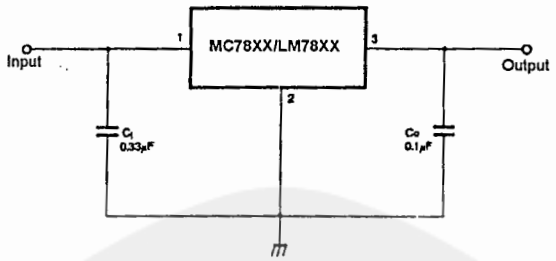


Figure 5. DC Parameters

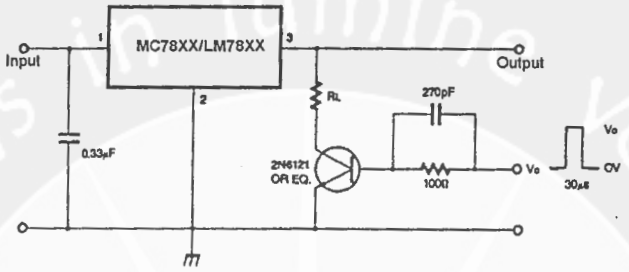


Figure 6. Load Regulation

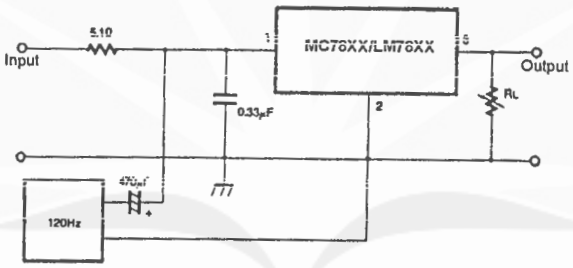


Figure 7. Ripple Rejection

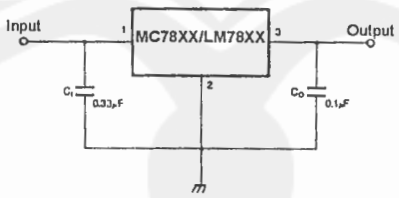
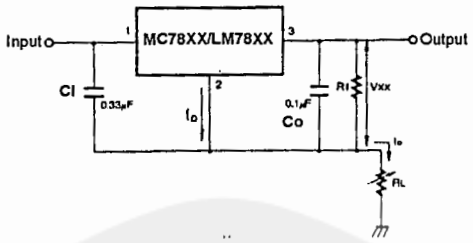


Figure 8. Fixed Output Regulator



$$I_o = \frac{V_{XX}}{R1} + I_Q$$

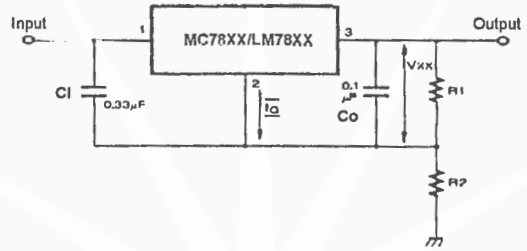
Figure 9. Constant Current Regulator

Notes:

(1) To specify an output voltage, substitute voltage value for "XX." A common ground is required between the input and the Output voltage. The input voltage must remain typically 2.0V above the output voltage even during the low point on the input ripple voltage.

(2) CI is required if regulator is located an appreciable distance from power Supply filter.

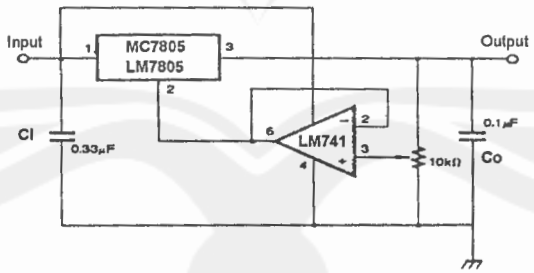
(3) CO improves stability and transient response.



$$I_{R1} \geq 5I_Q$$

$$V_O = V_{XX}(1+R_2/R_1)+I_QR_2$$

Figure 10. Circuit for Increasing Output Voltage



$$I_{R1} \geq 5\ I_Q$$

$$V_O = V_{XX}(1+R_2/R_1)+I_QR_2$$

Figure 11. Adjustable Output Regulator (7 to 30V)

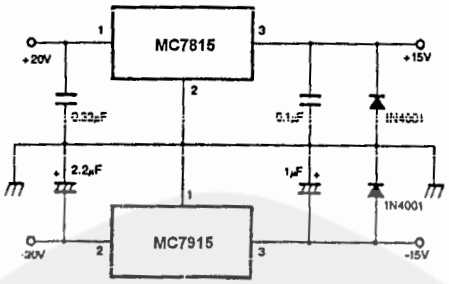


Figure 15. Split Power Supply (±15V-1A)

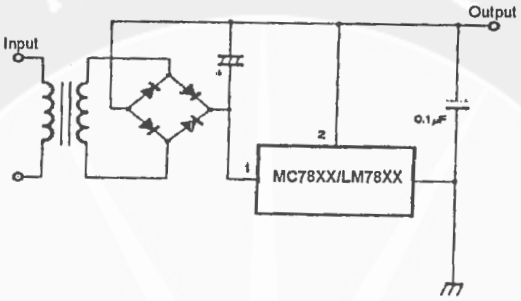


Figure 16. Negative Output Voltage Circuit

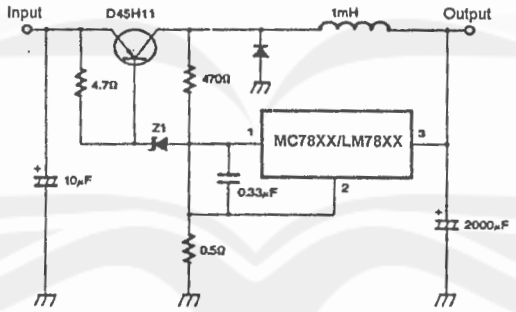
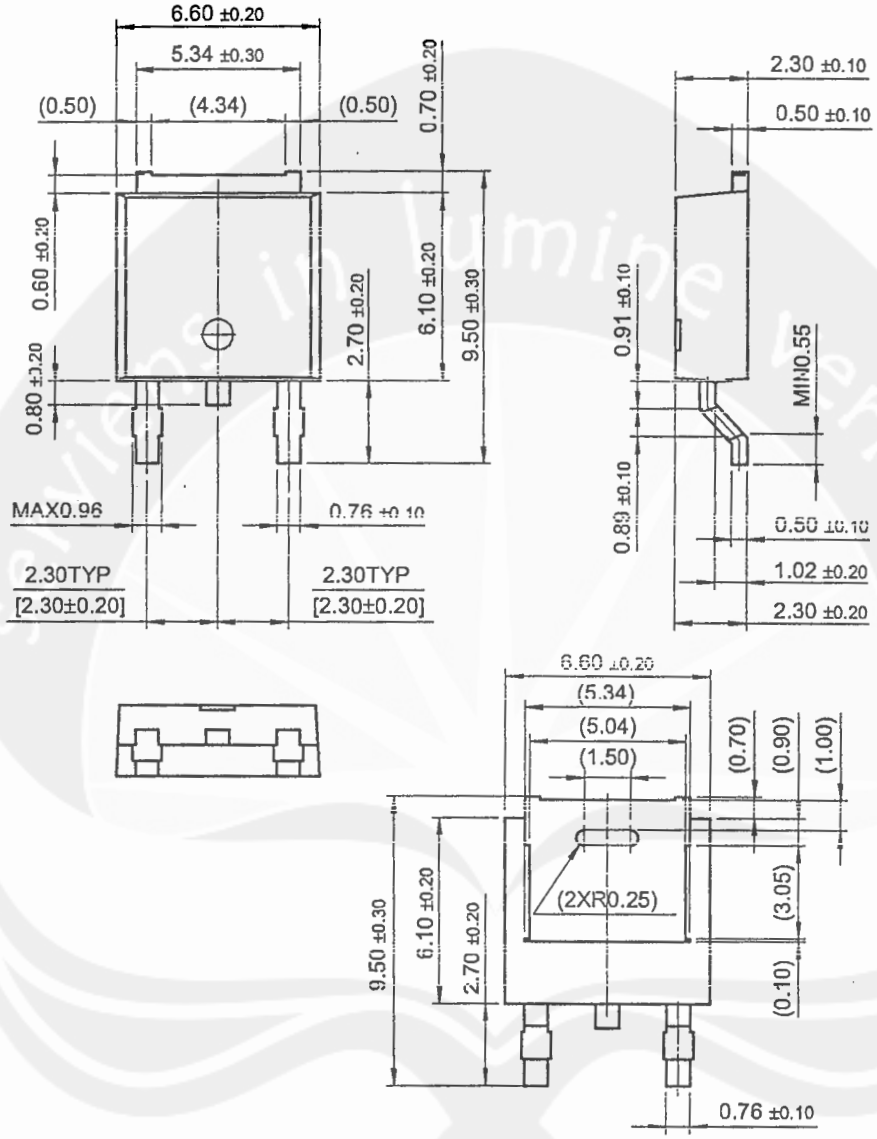


Figure 17. Switching Regulator

Mechancal Dimensions (Continued)

Package

D-PAK



Ordering Information

Product Number	Output Voltage Tolerance	Package	Operating Temperature
LM7805CT	±4%	TO-220	0 ~ + 125°C

Product Number	Output Voltage Tolerance	Package	Operating Temperature
MC7805CT	±4%	TO-220	0 ~ + 125°C
MC7806CT			
MC7808CT			
MC7809CT			
MC7810CT			
MC7812CT			
MC7815CT			
MC7818CT			
MC7824CT			
MC7805CDT		D-PAK	
MC7806CDT			
MC7808CDT			
MC7809CDT			
MC7810CDT			
MC7812CDT			
MC7805ACT	±2%	TO-220	
MC7806ACT			
MC7808ACT			
MC7809ACT			
MC7810ACT			
MC7812ACT			
MC7815ACT			
MC7818ACT			
MC7824ACT			

LAMPIRAN 4

Data Sheet IC ULN2803

MOTOROLA

ULN2803
ULN2804

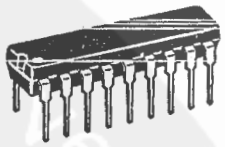
Octal High Voltage, High Current Darlington Transistor Arrays

The eight NPN Darlington connected transistors in this family of arrays are ideally suited for interfacing between low logic level digital circuitry (such as TTL, CMOS or PMOS/NMOS) and the higher current/voltage requirements of lamps, relays, printer hammers or other similar loads for a broad range of computer, industrial, and consumer applications. All devices feature open–collector outputs and free wheeling clamp diodes for transient suppression.

The ULN2803 is designed to be compatible with standard TTL families while the ULN2804 is optimized for 6 to 15 volt high level CMOS or PMOS.

OCTAL PERIPHERAL DRIVER ARRAYS

SEMICONDUCTOR TECHNICAL DATA



A SUFFIX
PLASTIC PACKAGE
CASE 707

MAXIMUM RATINGS (T_A = 25°C and rating apply to any one device in the package, unless otherwise noted.)

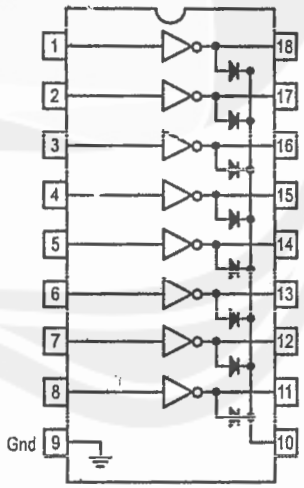
Rating	Symbol	Value	Unit
Output Voltage	V_O	50	V
Input Voltage (Except ULN2801)	V_I	30	V
Collector Current – Continuous	I_C	500	mA
Base Current – Continuous	I_B	25	mA
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	–55 to +150	°C
Junction Temperature	T_J	125	°C

$R_{\theta JA}$ = 55°C/W
Do not exceed maximum current limit per driver.

ORDERING INFORMATION

Device	Characteristics		
	Input Compatibility	V_{CE}(Max)/I_C(Max)	Operating Temperature Range
ULN2803A ULN2804A	TTL, 5.0 V CMOS 6 to 15 V CMOS, PMOS	50 V/500 mA	T_A = 0 to + 70°C

PIN CONNECTIONS



TEST FIGURES

(See Figure Numbers in Electrical Characteristics Table)

Figure 1.

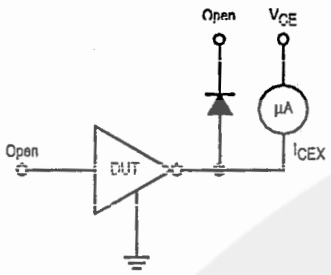


Figure 2.

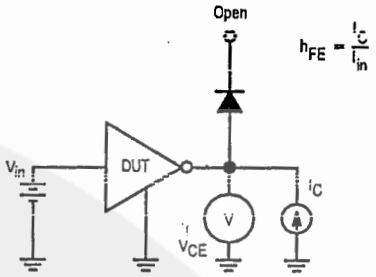


Figure 3.

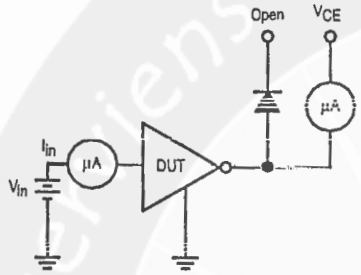


Figure 4.

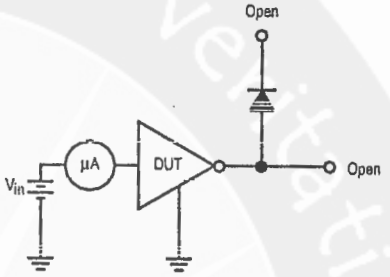


Figure 5.

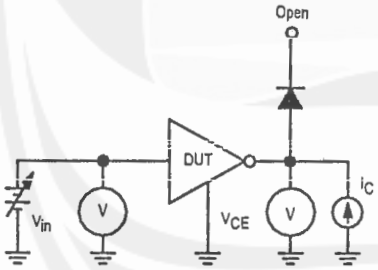


Figure 6.

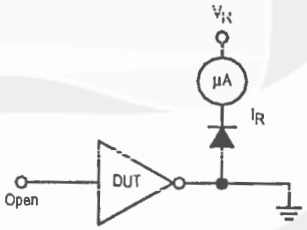
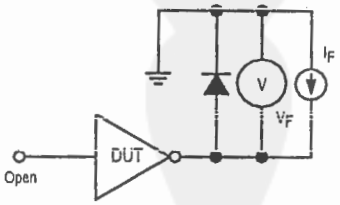


Figure 7.



TYPICAL CHARACTERISTIC CURVES – T_A = 25°C, unless otherwise noted

Output Characteristics

Figure 8. Output Current versus Saturation Voltage

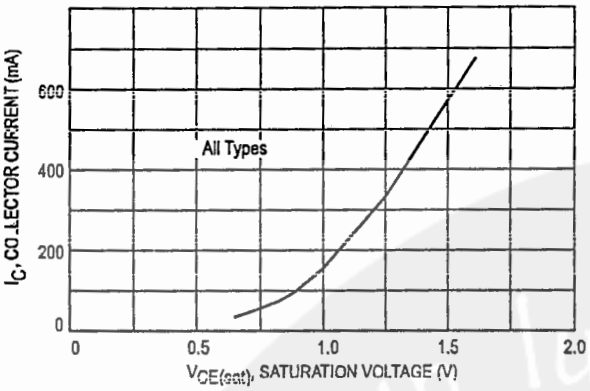
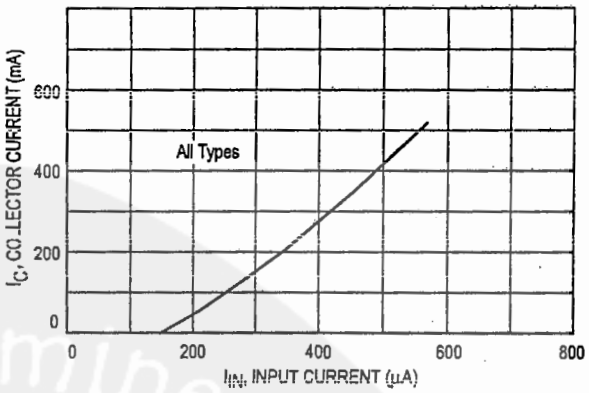


Figure 9. Output Current versus Input Current



Input Characteristics

Figure 10. ULN2803 Input Current versus Input Voltage

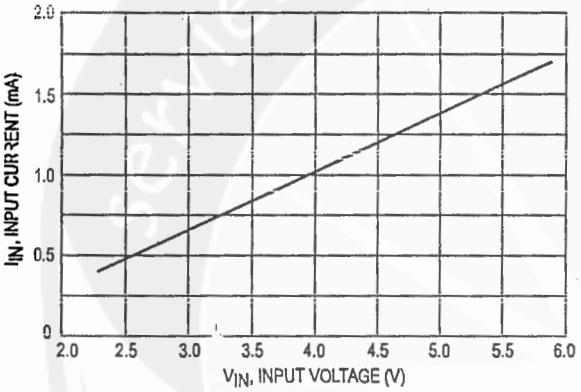


Figure 11. ULN2804 Input Current versus Input Voltage

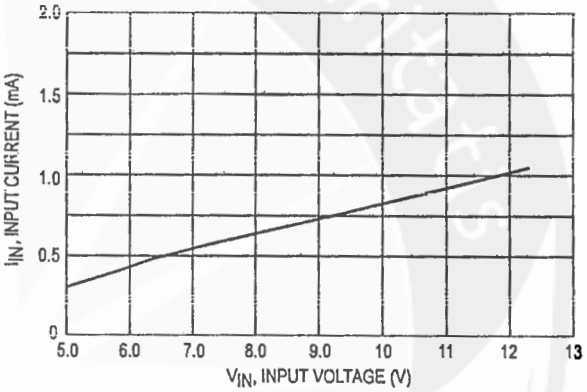
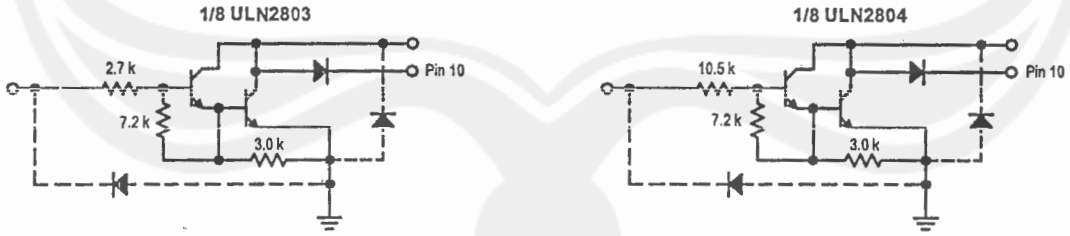
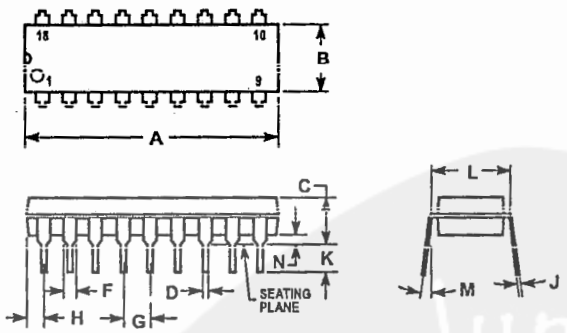


Figure 12. Representative Schematic Diagrams



OUTLINE DIMENSIONS

A SUFFIX
PLASTIC PACKAGE
CASE 707–02
ISSUE C



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.55	4.57	0.140	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

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ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298

MOTOROLA

LAMPIRAN 5

Data Sheet
MJ15025

PNP - MJ15023, MJ15025*

*MJ15025 is a Preferred Device

Silicon Power Transistors

The MJ15023 and MJ15025 are PowerBase power transistors designed for high power audio, disk head positioners and other linear applications.

Features

- High Safe Operating Area (100% Tested) −2 A @ 80 V
- High DC Current Gain − h_{FE} = 15 (Min) @ I_C = 8 Adc
- Pb−Free Packages are Available*

ON Semiconductor®

http://onsemi.com

16 AMPERES
SILICON POWER TRANSISTORS
200 − 250 VOLTS, 250 WATTS

TO−204AA (TO−3)
CASE 1−07
STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage MJ15023 MJ15025	V_{CEO}	 200 250	Vdc
Collector−Base Voltage MJ15023 MJ15025	V_{CBO}	 350 400	Vdc
Emitter−Base Voltage	V_{EBO}	5	Vdc
Collector−Emitter Voltage	V_{CEX}	400	Vdc
Collector Current − Continuous − Peak (Note 1)	I_C	16 30	Adc
Base Current − Continuous	I_B	5	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	250 1.43	W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200	°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	0.70	°C/W

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

MARKING DIAGRAM

MJ1502x = Device Code
x = 3 or 5
G = Pb−Free Package
A = Assembly Location
Y = Year
WW = Work Week
MEX = Country of Origin

ORDERING INFORMATION

Device	Package	Shipping
MJ15023	TO−204	100 Units / Tray
MJ15023G	TO−204 (Pb−Free)	100 Units / Tray
MJ15025	TO−204	100 Units / Tray
MJ15025G	TO−204 (Pb−Free)	100 Units / Tray

Preferred devices are recommended choices for future use and best overall value.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

February, 2006 − Rev. 10

Publication Order Number:
MJ15023/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (Note 2) (I_C = 100 mAdc, I_B = 0)	MJ15023 MJ15025	$V_{CEO(sus)}$	 200 250	 – –	–
Collector Cutoff Current (V_{CE} = 200 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 250 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	 MJ15023 MJ15025	I_{CEX}	 – –	 250 250	μAdc
Collector Cutoff Current (V_{CE} = 150 Vdc, I_B = 0) (V_{CE} = 200 Vdc, I_B = 0)	 MJ15023 MJ15025	I_{CEO}	 – –	 500 500	μAdc
Emitter Cutoff Current (V_{CE} = 5 Vdc, I_B = 0)	Both	I_{EBO}	–	500	μAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased (V_{CE} = 50 Vdc, t = 0.5 s (non-repetitive)) (V_{CE} = 80 Vdc, t = 0.5 s (non-repetitive))		$I_{S/b}$	 5 2	 – –	Adc
ON CHARACTERISTICS					
DC Current Gain (I_C = 8 Adc, V_{CE} = 4 Vdc) (I_C = 16 Adc, V_{CE} = 4 Vdc)		h_{FE}	 15 5	 60 –	–
Collector–Emitter Saturation Voltage (I_C = 8 Adc, I_B = 0.8 Adc) (I_C = 16 Adc, I_B = 3.2 Adc)		$V_{CE(sat)}$	 – –	 1.4 4.0	Vdc
Base–Emitter On Voltage (I_C = 8 Adc, V_{CE} = 4 Vdc)		$V_{BE(on)}$	–	2.2	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain – Bandwidth Product (I_C = 1 Adc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)		f_T	4	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)		C_{ob}	–	600	pF

2. Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

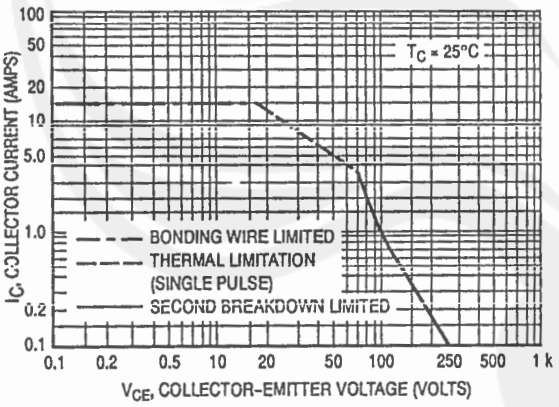


Figure 1. Active–Region Safe Operating Area

There are two limitations on the powerhandling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

TYPICAL CHARACTERISTICS

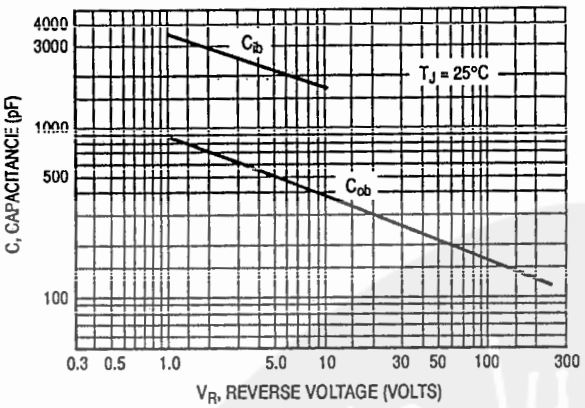


Figure 2. Capacitances

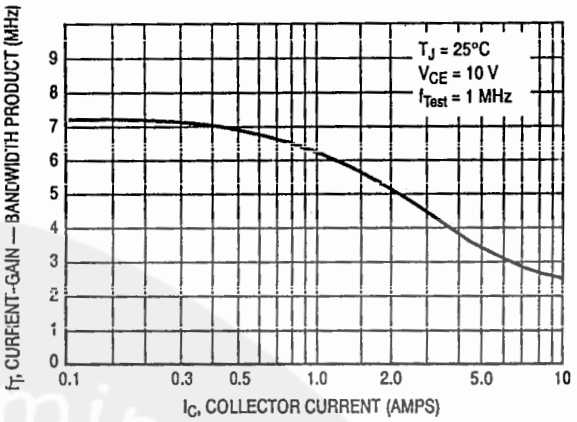


Figure 3. Current–Gain — Bandwidth Product

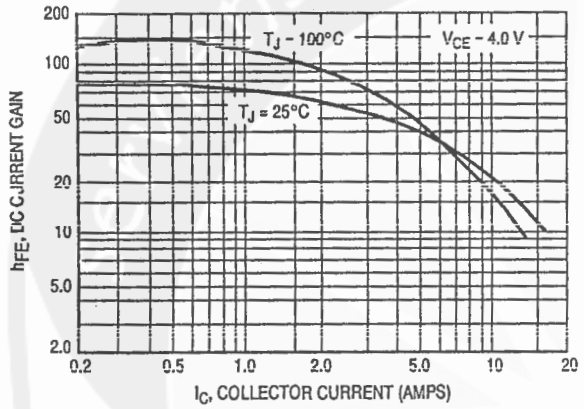


Figure 4. DC Current Gain

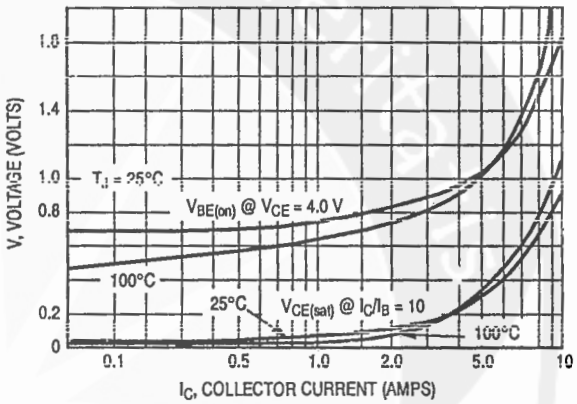
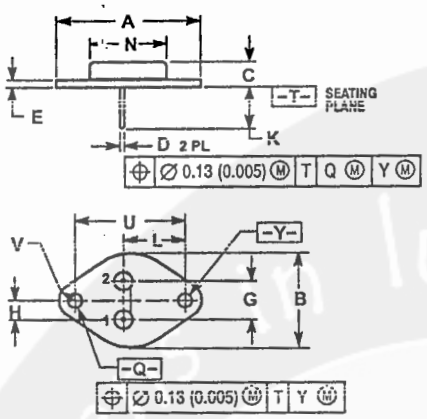


Figure 5. "On" Voltages

PACKAGE DIMENSIONS

TO–204 (TO–3)
CASE 1–07
ISSUE Z



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH *REFERENCED TO-204AA OUTLINE* SHALL APPLY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.550 REF		39.37 REF	
B	---	1.050	---	26.67
C	0.250	0.335	6.35	8.51
D	0.038	0.043	0.97	1.09
E	0.055	0.070	1.40	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	---	0.830	---	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

PUBLICATION ORDERING INFORMATION

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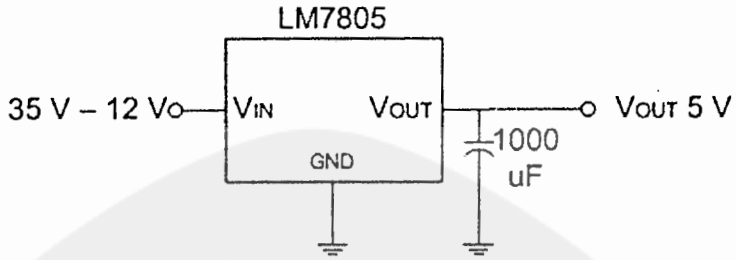
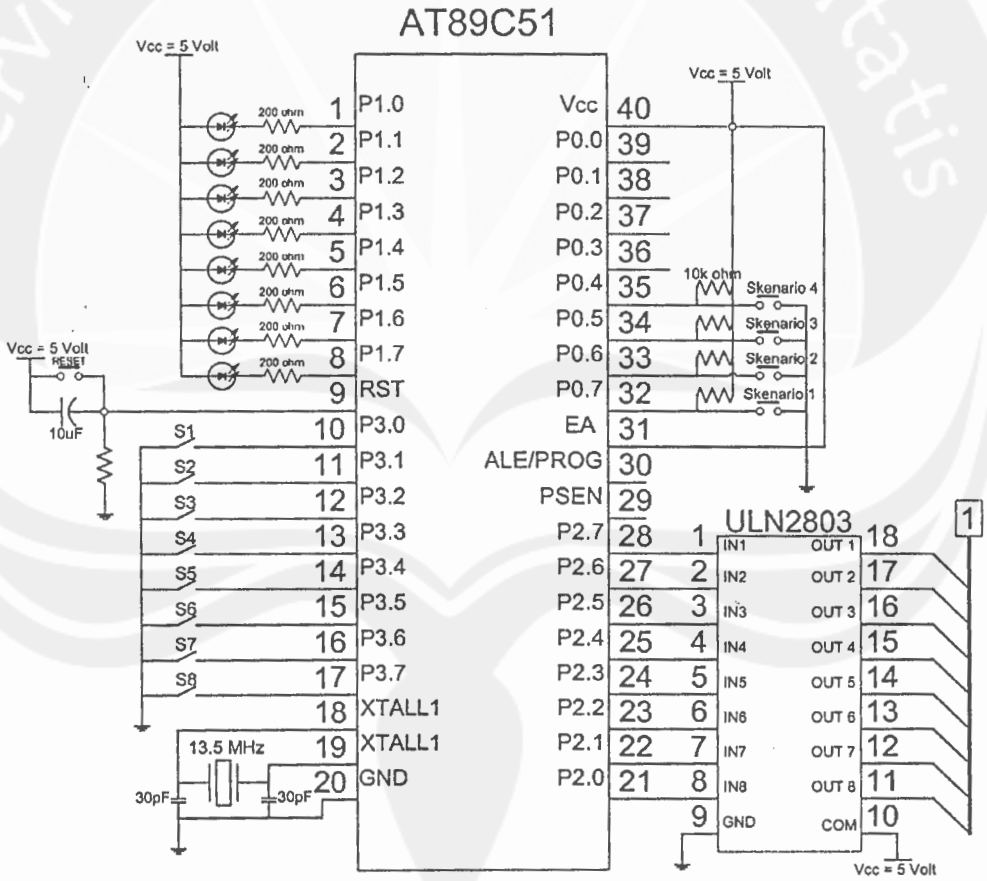
MJ15023/D

LAMPIRAN 6

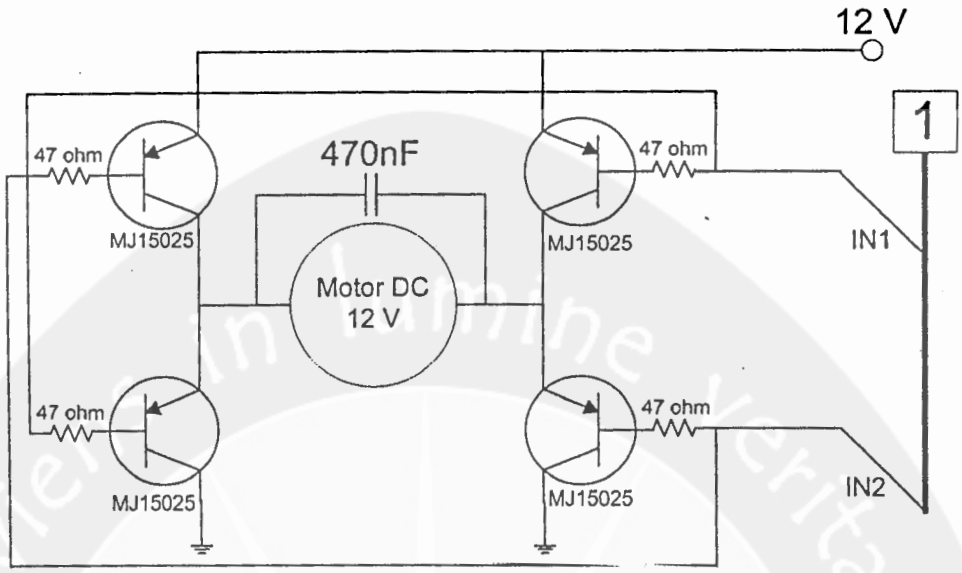
Skema Rangkaian



Gambar Rangkaian *IC* Regulator



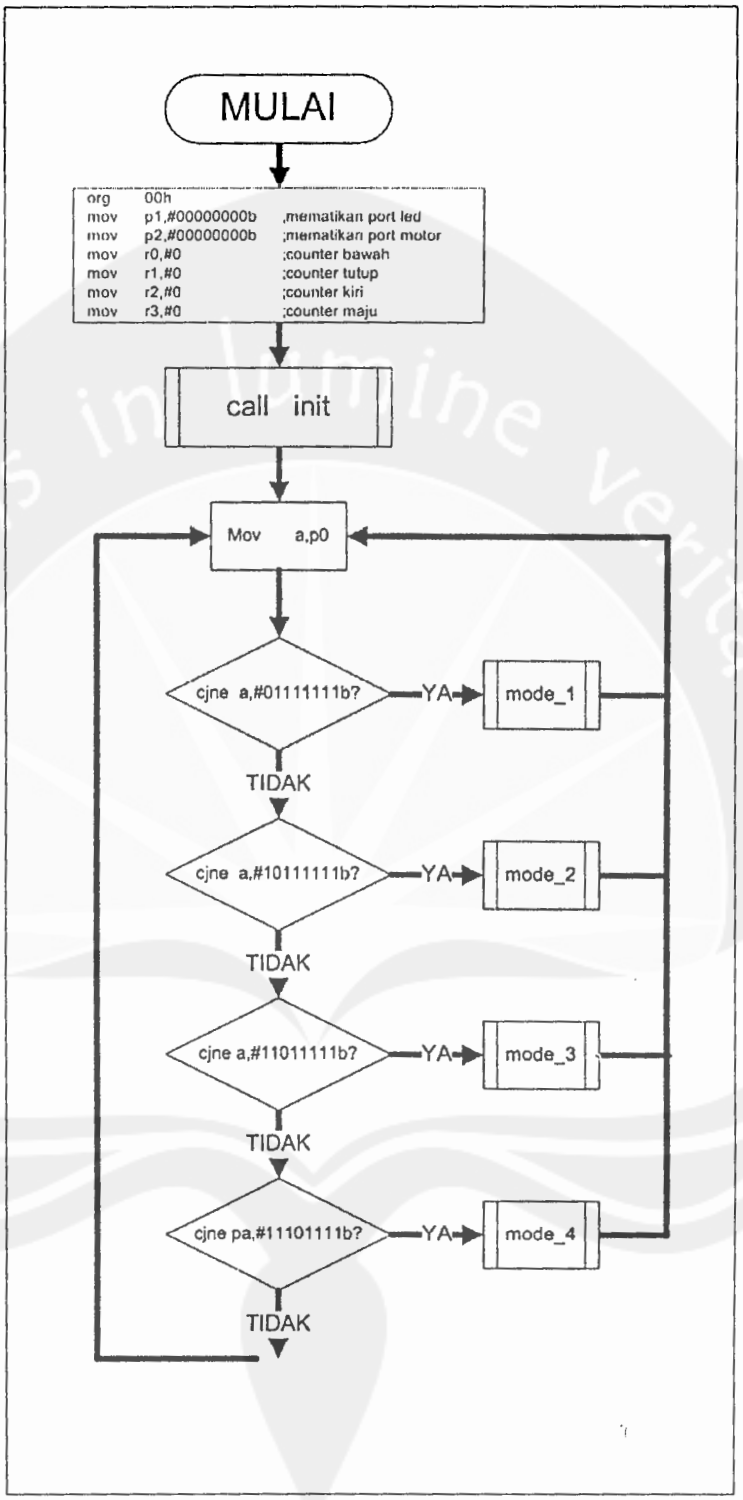
Gambar Rangkaian Mikrokontroler



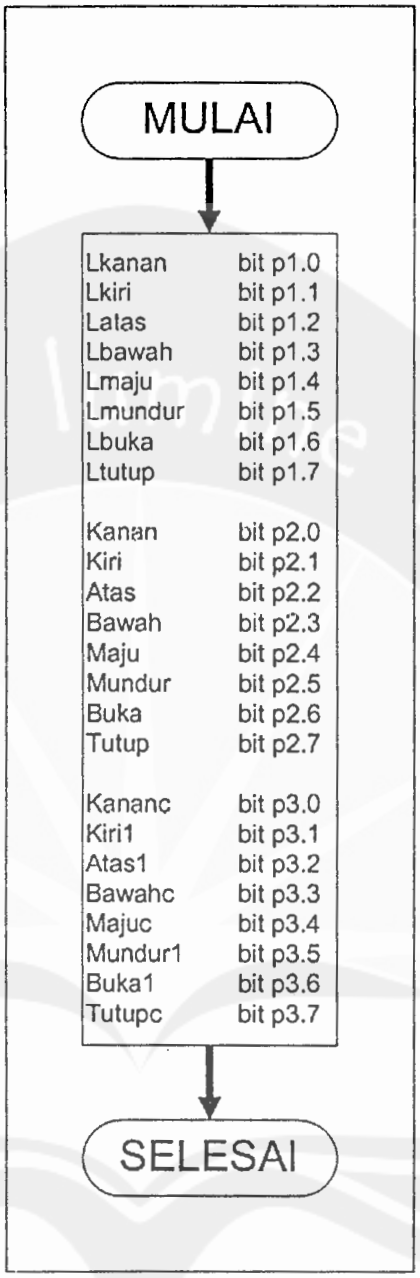
Gambar Rangkaian *Driver*

LAMPIRAN 7

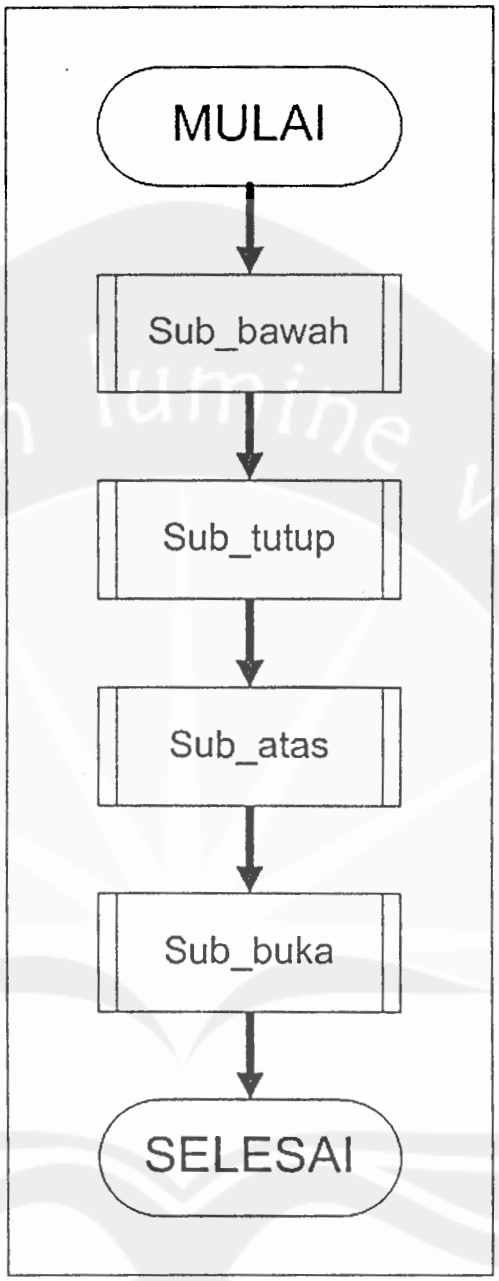
Diagram Alir Program



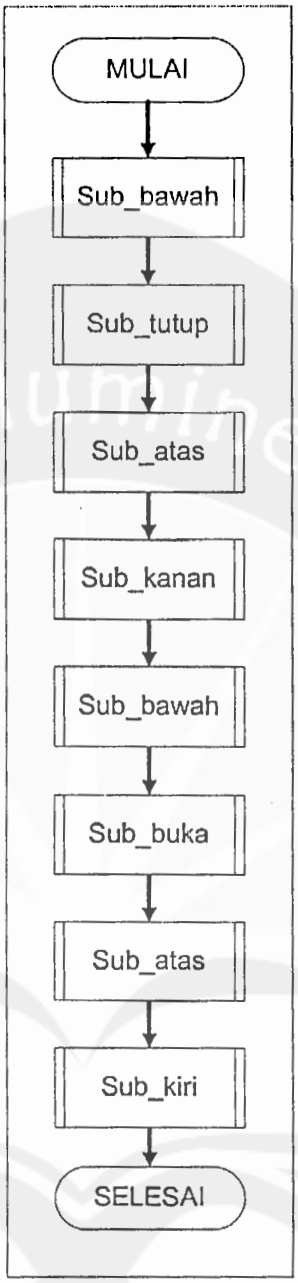
Gambar Diagram Alir Program Utama



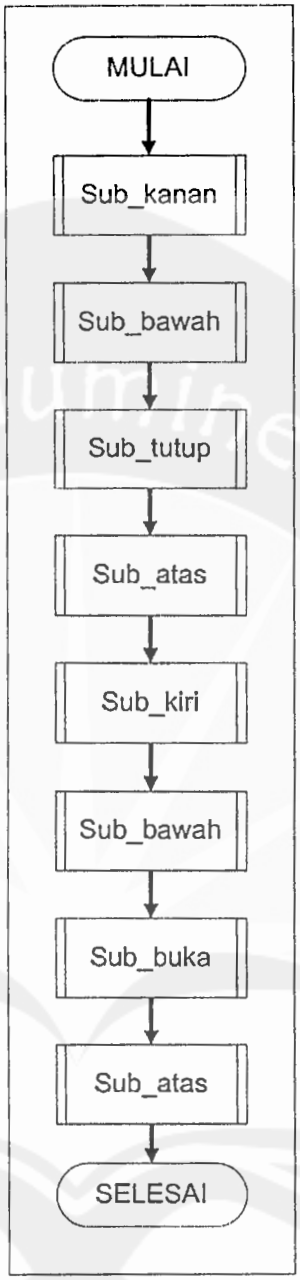
Gambar Diagram Alir Inisialisasi Port



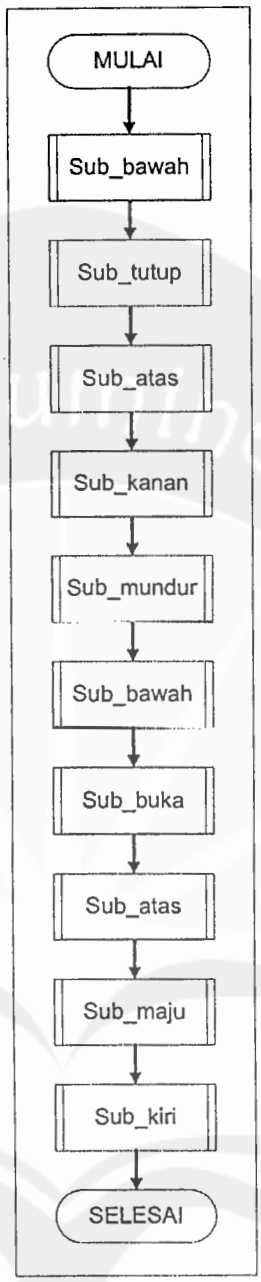
Gambar Diagram Alir Gerakan Skenario 1



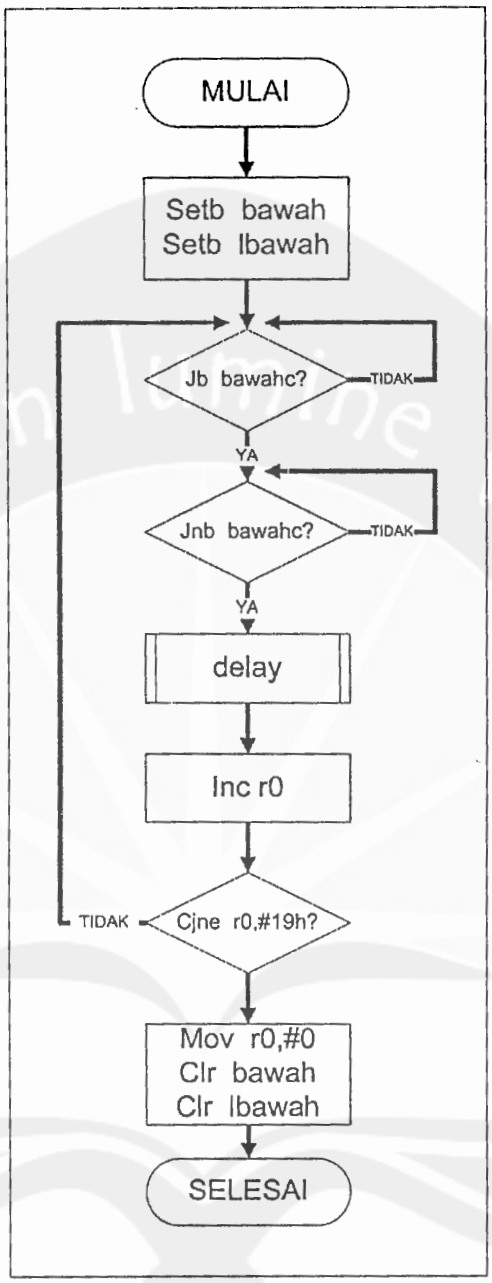
Gambar Diagram Alir Gerakan Skenario 2



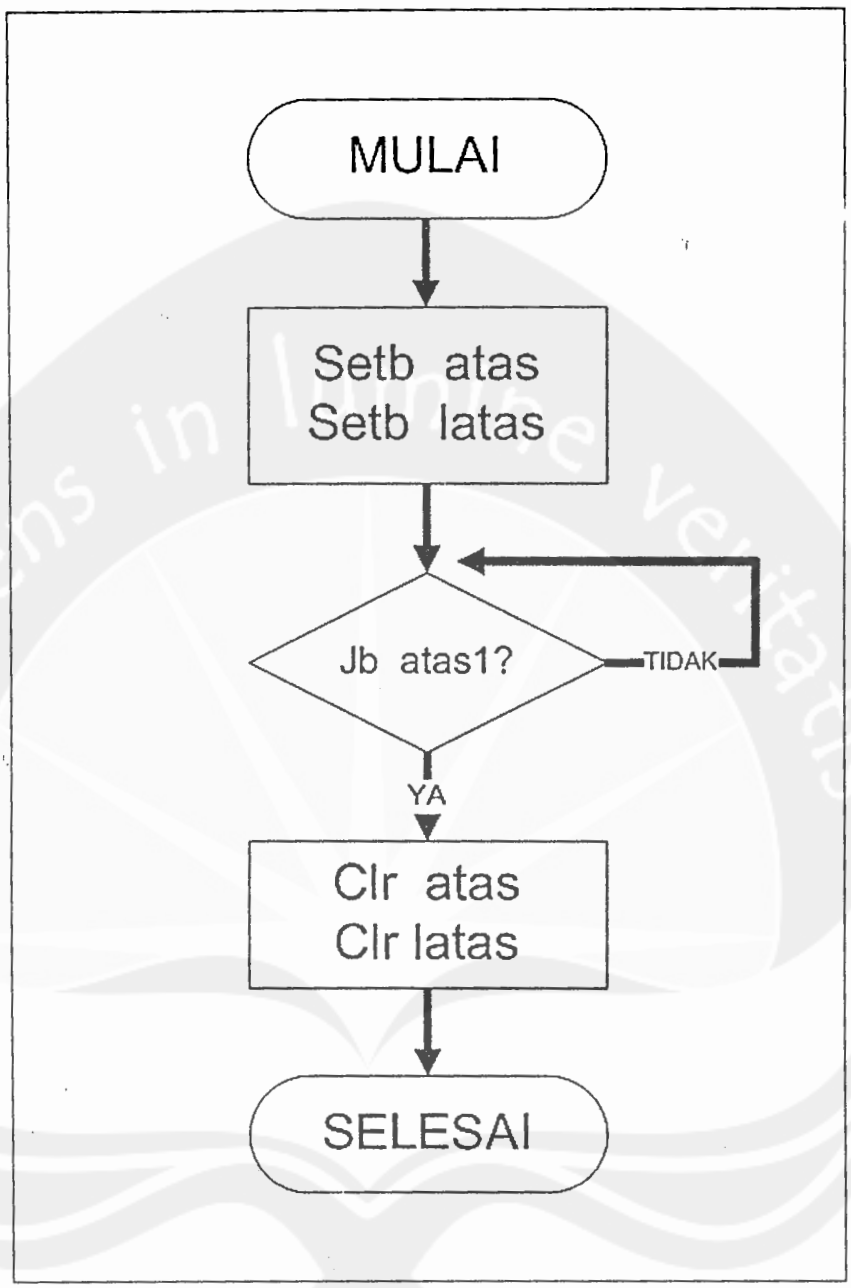
Gambar Diagram Alir Gerakan Skenario 3



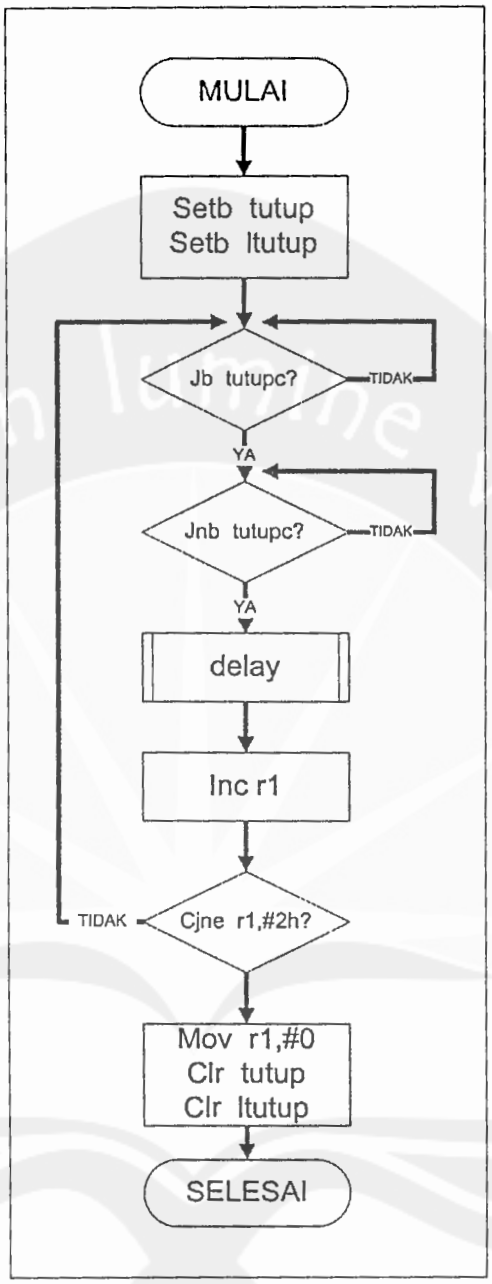
Gambar Diagram Alir Gerakan Skenario 4



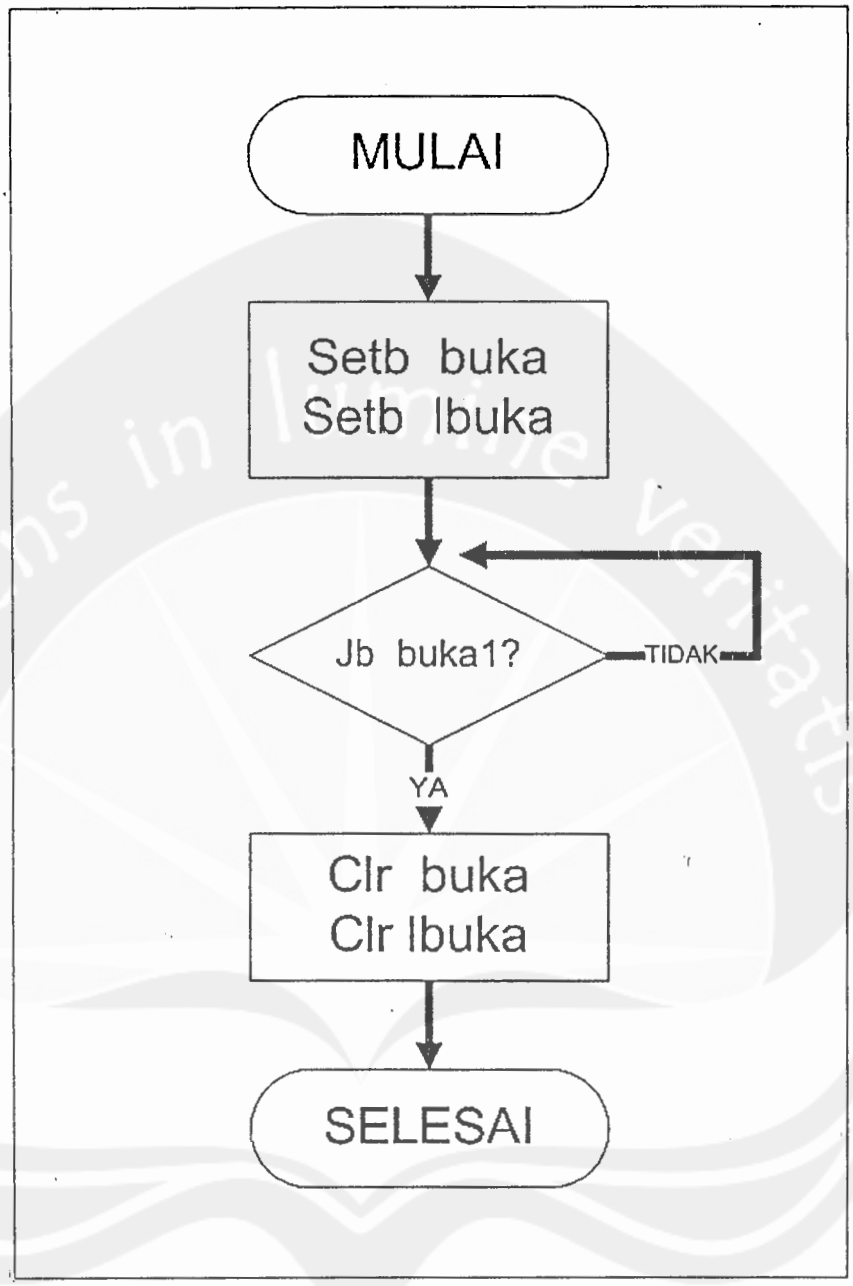
Gambar Diagram Alir Gerakan Lengan ke Bawah



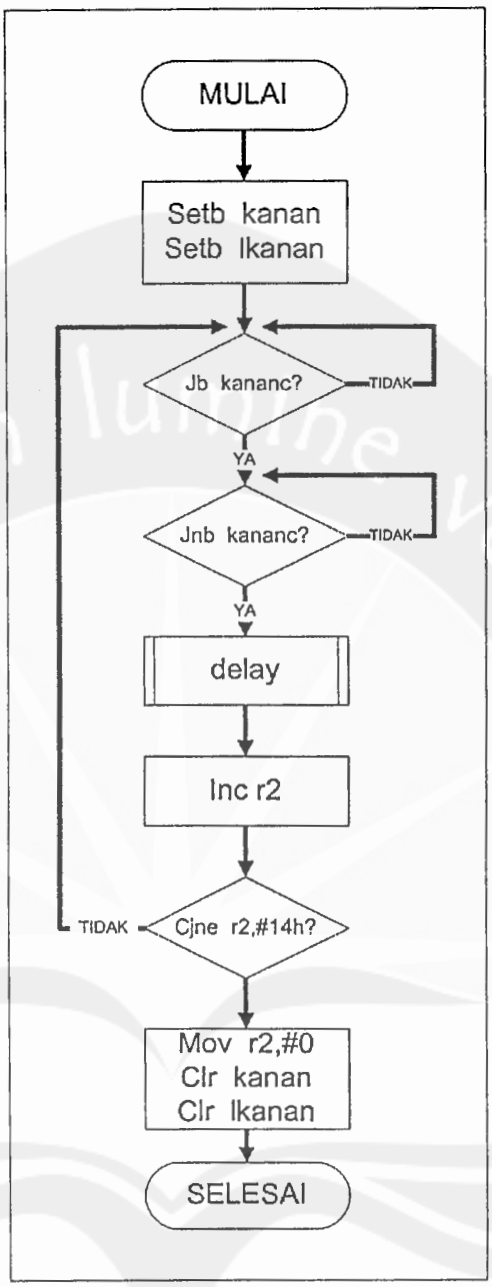
Gambar Diagram Alir Gerakan Lengan ke Atas



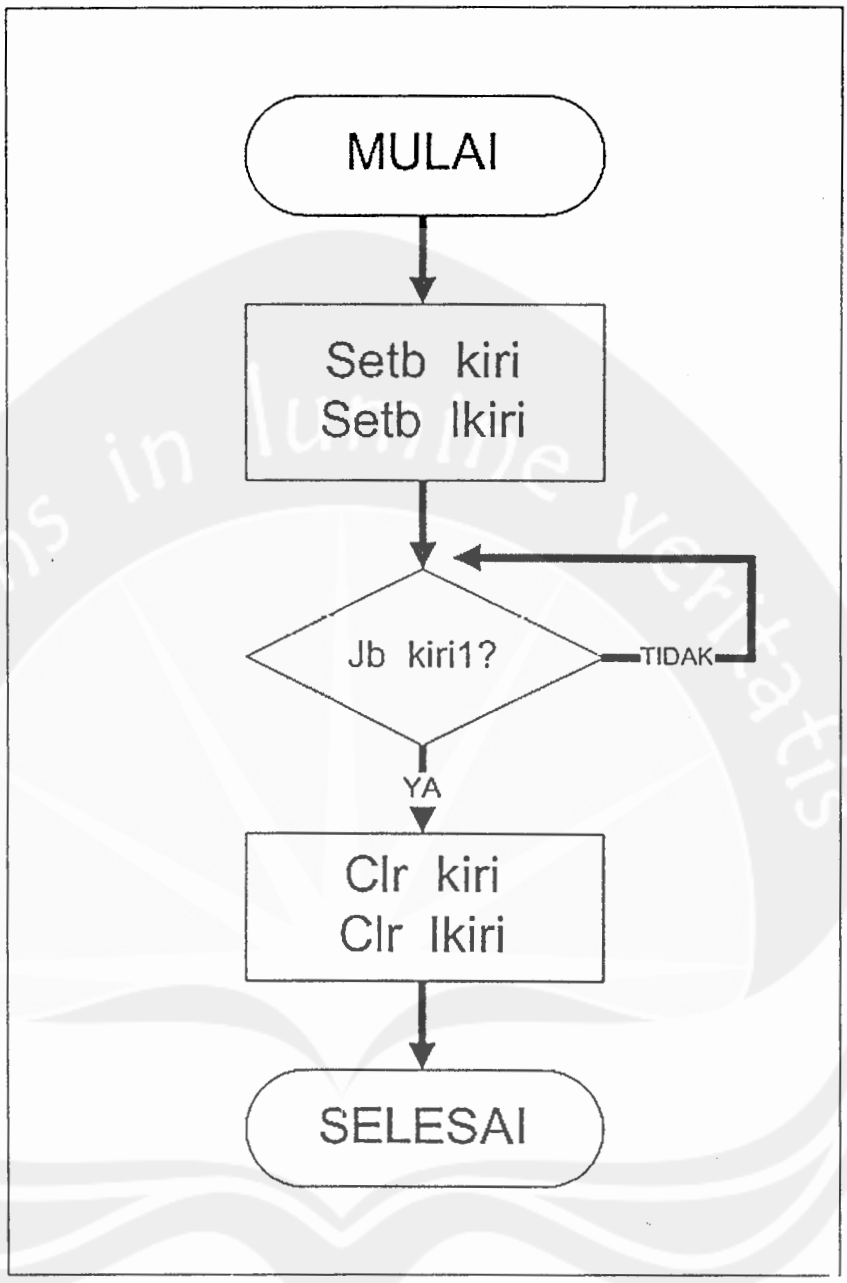
Gambar Diagram Alir Gerakan *Gripper* Menutup



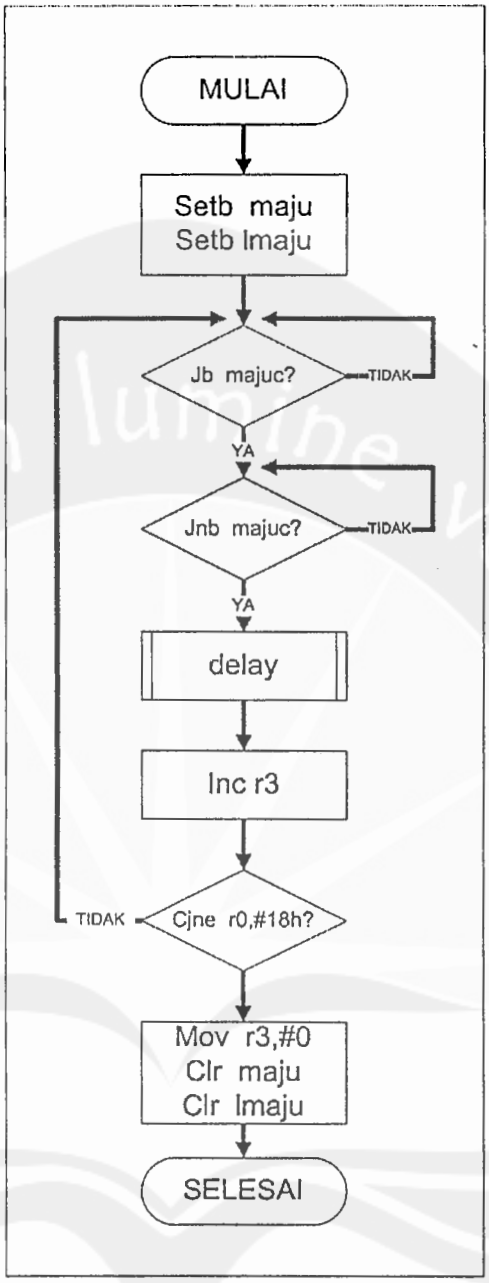
Gambar Diagram Alir Gerakan *Gripper* Membuka



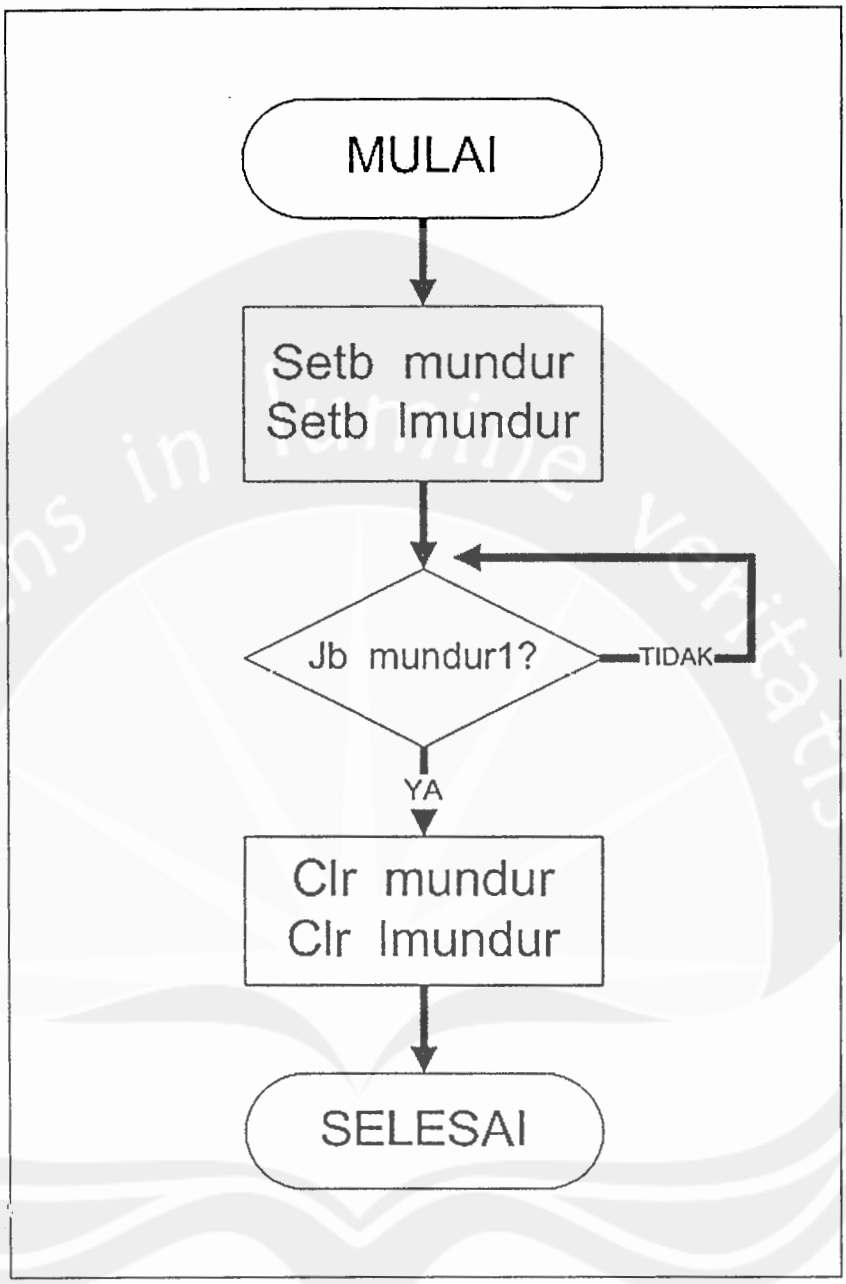
Gambar Diagram Alir Gerakan Lengan ke Kanan



Gambar Diagram Alir Gerakan Lengan ke Kiri



Gambar Diagram Alir Gerakan Lengan Maju



Gambar Diagram Alir Gerakan Lengan Mundur

LAMPIRAN 8

Listing Program

```
;=========================================================
;                    Mempersiapkan Memori
;=========================================================
org  00h
mov  p1,#00000000b  ;mematikan port led
mov  p2,#00000000b  ;mematikan port motor
mov  r0,#0          ;counter bawah
mov  r1,#0          ;counter tutup
mov  r2,#0          ;counter kiri
mov  r3,#0          ;counter maju
;---------------------------------------------------------

call init      ;memanggil sub_rutin init

;=========================================================
;                    Memilih Mode Gerakan
;=========================================================

start:
     mov  a,p0
next1:
     cjne a,#01111111b,next2
     call mode_1
     sjmp start
next2:
     cjne a,#10111111b,next3
     call mode_2
     sjmp start
next3:
     cjne a,#11011111b,next4
     call mode_3
     sjmp start
```

```
next4:
      cjne a,#11101111b,start
      call mode_4
      sjmp start
;-------------------------------------------------------

init:
;=======================================================
;          Inisialisasi Port 1 sebagai Port Led
;=======================================================
lkanan    bit p1.0
lkiri     bit p1.1
latas     bit p1.2
lbawah    bit p1.3
lmaju     bit p1.4
lmundur   bit p1.5
lbuka     bit p1.6
ltutup    bit p1.7

;=======================================================
;          Inisialisasi Port 2 sebagai Port Motor
;=======================================================
kanan     bit p2.0
kiri      bit p2.1
atas      bit p2.2
bawah     bit p2.3
maju      bit p2.4
mundur    bit p2.5
buka      bit p2.6
tutup     bit p2.7
```

```
;=========================================================
;         Inisialisasi Port 3 sebagai Port Switch
;=========================================================
kananc    bit p3.0
kiri1     bit p3.1
atas1     bit p3.2
bawahc    bit p3.3
majuc     bit p3.4
mundur1   bit p3.5
buka1     bit p3.6
tutupc    bit p3.7
;---------------------------------------------------------
Ret

mode_1:
;=========================================================
;                              Mode 1
;=========================================================
call sub_bawah
call delay
call sub_tutup
call delay
call sub_atas
call delay
call sub_buka
call delay
;---------------------------------------------------------
ret
```

```
mode_2:
;=====================================================
;                          Mode2
;=====================================================
call sub_bawah
call delay
call sub_tutup
call delay
call sub_atas
call delay
call sub_kanan
call delay
call sub_bawah
call delay
call sub_buka
call delay
call sub_atas
call delay
call sub_kiri
call delay
;-----------------------------------------------------
ret

mode_3:
;=====================================================
;                          Mode 3
;=====================================================
call sub_kanan
call delay
call sub_bawah
call delay
call sub_tutup
```

```
call delay
call sub_atas
call delay
call sub_kiri
call delay
call sub_bawah
call delay
call sub_buka
call delay
call sub_atas
call delay
;-------------------------------------------------------
ret

mode_4:
;=======================================================
;                          Mode 4
;=======================================================
call sub_bawah
call delay
call sub_tutup
call delay
call sub_atas
call delay
call sub_kanan
call delay
call sub_mundur
call delay
call sub_bawah
call delay
call sub_buka
call delay
```

```
call sub_atas
call delay
call sub_maju
call delay
call sub_kiri
call delay
;-------------------------------------------------------
Ret

sub_bawah:
;=======================================================
;                    Gerakan ke Bawah
;=======================================================
     setb bawah
cek1:
     jb   bawahc,cek1
wait1:
     jnb  bawahc,wait1
     call delay
     inc  r0              ;counter bawah
     cjne r0,#96h,cek1    ;counter=150
     mov  r0,#0           ;mengembalikan nilai r0
     clr  bawah
;-------------------------------------------------------
ret

sub_atas:
;=======================================================
;                     Gerakan ke Atas
;=======================================================
     setb atas
cek2:
```

```
sub_maju:
;=======================================================
;                    Gerakan Lengan Maju
;=======================================================
     setb maju
cek7:
     jb   majuc,cek7
wait7:
     jnb  majuc,wait7
     call delay
     inc  r3              ;counter kanan
     cjne r3,#3Ch,cek7    ;counter=60
     mov  r3,#0           ;mengembalikan nilai r3
     clr  maju
;-------------------------------------------------------
ret

sub_mundur:
;=======================================================
;                  Gerakan Lengan Mundur
;=======================================================
     setb mundur
cek8:
     jb   mundur1,cek8
     clr  mundur
;-------------------------------------------------------
ret
```

```
     jb   atas1,cek2
     clr  atas
;-------------------------------------------------------
Ret

sub_tutup:
;=======================================================
;                  Gerakan Menutup Gripper
;=======================================================
     setb tutup
cek3:
     jb   tutupc,cek3
wait3:
     jnb  tutupc,wait3
     call delay
     inc  r1              ;counter tutup
     cjne r1,#1Bh,cek3    ;counter=27
     mov  r1,#0           ;mengembalikan nilai r1
     clr  tutup
;-------------------------------------------------------
ret

sub_buka:
;=======================================================
;                Gerakan Membuka Gripper
;=======================================================
     setb buka
cek4:
     jb   buka1,cek4
     clr  buka
;-------------------------------------------------------
ret
```

```
sub_kanan:
;=========================================================
;                   Gerakan Lengan ke Kanan
;=========================================================
     setb kanan
cek5:
     jb   kananc,cek5
wait5:
     jnb  kananc,wait5
     call delay
     inc  r2              ;counter kanan
     cjne r2,#48h,cek5    ;counter=72
     mov  r2,#0           ;mengembalikan nilai r2
     clr  kanan
;---------------------------------------------------------
ret

sub_kiri:
;=========================================================
;                   Gerakan Lengan ke Kiri
;=========================================================
     setb kiri
cek6:
     jb   kiri1,cek6
     clr  kiri
;---------------------------------------------------------
Ret
```

```
delay:    mov r6,#3
delay1:   mov r7,#0
          djnz r7,$
          djnz r6,delay1
ret
```

LAMPIRAN 9

Tabel Hasil Pengamatan Kepresisian *Counter* Target terhadap *Counter* Hasil

Tabel Hasil Pengamatan

Kepresisian *Counter* Target terhadap *Counter* Hasil

No.	Hasil Acak	Target		Hasil		Selisih *Clock*
		Panjang	*Clock*	Panjang	*Clock*	
1	2	30 mm	30	32 mm	32	2
2	4	37,5°	30	39°	31	1
3	3	30 mm	30	30 mm	30	0
4	1	22,5 mm	30	23 mm	30	0
5	1	22,5 mm	30	23 mm	30	0
6	4	37,5°	30	40°	32	2
7	3	30 mm	30	30 mm	30	0
8	2	30 mm	30	31 mm	31	1
9	4	37,5°	30	40°	32	2
10	1	22,5 mm	30	24 mm	32	2
11	3	30 mm	30	31 mm	31	1
12	4	37,5°	30	41°	33	3
13	2	30 mm	30	32 mm	32	2
14	1	22,5 mm	30	23,5 mm	31	1
15	3	30 mm	30	30 mm	30	0
16	2	30 mm	30	30 mm	30	0
17	4	37,5°	30	40°	32	2
18	4	37,5°	30	39°	31	1
19	4	37,5°	30	41°	33	3
20	2	30 mm	30	30 mm	30	0
21	1	22,5 mm	30	23,5 mm	31	1
22	3	30 mm	30	32 mm	32	2
23	2	30 mm	30	33 mm	33	3
24	1	22,5 mm	30	23,5 mm	31	1
25	4	37,5°	30	39°	31	1

Tabel (Lanjutan) Hasil Pengamatan

Kepresisian *Counter* Target terhadap *Counter* Hasil

26	2	30 mm	30	31 mm	32	1
27	2	30 mm	30	31 mm	32	1
28	1	22,5 mm	30	22,5 mm	30	0
29	3	30 mm	30	30 mm	30	0
30	1	22,5 mm	30	25 mm	33	3
			ΣX			36

LAMPIRAN 10

Tabel Analisis Data Kepresisian *Counter* Target terhadap *Counter* Hasil

Tabel Analisis Data

Kepresisian *Counter* Target terhadap *Counter* Hasil

Nilai Data (X)	$(X-\overline{X})=x$	$(X-\overline{X})^2=x^2$
2	0,8	0,64
1	-0,2	0,04
0	0	0
0	0	0
0	0	0
2	0,8	0,64
0	0	0
1	-0,2	0,04
2	0,8	0,64
2	0,8	0,64
1	-0,2	0,04
3	1,8	3,24
2	0,8	0,64
1	-0,2	0,04
0	0	0
0	0	0
2	0,8	0,64
1	-0,2	0,04
3	1,8	3,24
0	0	0
1	-0,2	0,04
2	0,8	0,64
3	1,8	3,24
1	-0,2	0,04
1	-0,2	0,04
2	0,8	0,64

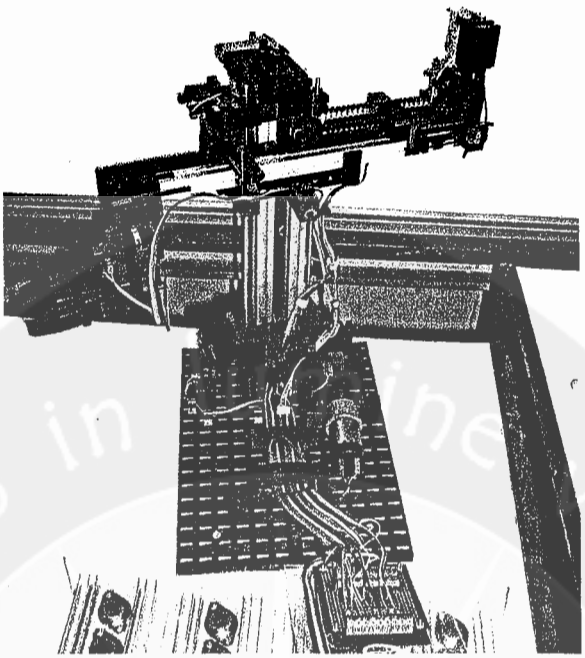
Tabel (Lanjutan) Analisis Data

Kepresisian *Counter* Target terhadap *Counter* Hasil

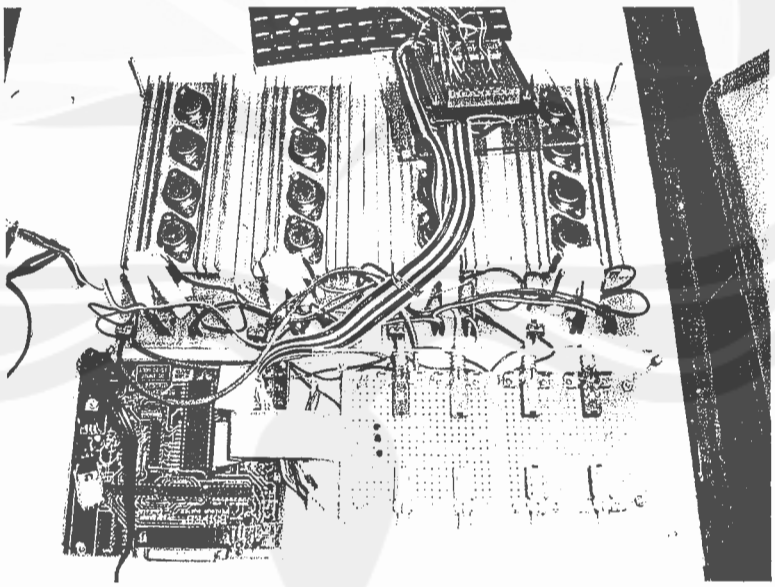
2	0,8	0,64
0	0	0
0	0	0
3	1,8	3,24
	$\sum(X-\overline{X})^2$	19,04

LAMPIRAN 11

Foto Pengendali
dan Model Robot Lengan Tiga Sumbu



Gambar Robot Lengan Tiga Sumbu



Gambar Rangkaian Pengendali