BAB 6

KESIMPULAN DAN SARAN

6.1. Kesimpulan

Dari perancangan sistem pengendalian peralatan listrik yang terintegrasi dengan perangkat *fixed telephone* berbasis mikrokontroler AT89S51 dapat ditarik kesimpulan bahwa sistem pengendali tersebut dapat berjalan dengan baik sesuai dengan tujuan dari penelitian ini, yaitu dapat mengendalikan beban yang terhubung dengan sistem pengendali. Pada penelitian ini, beban yang digunakan berupa lampu pijar. Fungsi pengendalian yang dilakukan sistem pengendali terhadap beban yang bekerja pada tegangan 220 volt AC berupa *ON* dan *OFF*. Berdasarkan uji coba yang dilakukan, sistem pengendali ini dapat menjalankan 17 prosedur yang dibagi menjadi 2 bagian dengan tingkat keberhasilan 100%.

Sistem ini bekerja dengan menggunakan jaringan telepon yang berfungsi sebagai mentransmisikan data, terutama pada pengendalian secara *remote*. Dalam pengendalian secara lokal, jaringan telepon berguna sebagai pengumpan yang kemudian sumber sinyalnya dihasilkan oleh tegangan 12 volt DC. Perangkat telepon yang digunakan untuk menjembatani perintah yang diberikan operator kepada sistem pengendali merupakan

perangkat telepon berjenis *fixed telephone*. Perangkat telepon yang digunakan harus mempunyai fitur DTMF (*Dual-Tone Multi-Frequency*) yang merupakan sumber input bagi sistem pengendali.

Sistem pengendali ini bekerja dalam dua kondisi, yaitu pengendalian secara *remote* dan pengendalian secara lokal. Pengendalian secara *remote* dapat diartikan bahwa operator dan sistem pengendali tidak berada pada lokasi yang sama. Operator harus melakukan panggilan ke nomor telepon yang terhubung dengan sistem pengendali untuk melakukan pengendalian, sehingga jaringan telepon mutlak dibutuhkan. Sedangkan pengendalian secara lokal dapat diartikan bahwa operator dan sistem pengendali berada pada lokasi yang sama, walaupun tidak selalu berdekatan. Dalam pengendalian ini tidak perlu melakukan panggilan karena operator sudah terhubung sistem pengendali melalui perangkat *fixed telephone*.

Walaupun sistem pengendali ini bekerja dalam dua kondisi, namun prosedur pengendaliannya sama. Operator perlu memasukkan *password* terlebih dahulu sebelum melakukan pengendalian. Pemberian input dilakukan dengan menekan tombol pada perangkat telepon. Terdapat umpan balik berupa nada yang dihasilkan sistem pengendali. Hanya ada sedikit perbedaan pada bagian umpan balik, yang berkaitan dengan perbedaan lokasi dalam melakukan pengendalian.

Perancangan ini menggunakan mikrokontroler seri AT89S51 karena memiliki beberapa keunggulan dan sesuai dengan kebutuhan, antara lain seperti kapasitas memori sebesar 4 kB, memiliki fitur ISP (*In-System*

Programming), harga yang murah, mudah diperoleh dan mudah dipahami sistem kerjanya. *Software* komputer yang digunakan dalam perancangan adalah BASCOM-8051. *Software* ini cukup sederhana sehingga mudah digunakan dan memiliki beberapa fitur yang cukup lengkap. *Software* ini menggunakan bahasa pemrograman BASIC dalam melakukan pengembangan perangkat lunak mikrokontroler. Selain itu, *software* ini dapat diperoleh dengan gratis walaupun dengan beberapa fitur yang dibatasi.

6.2. Saran

Berdasarkan hasil penelitian, sistem pengendali yang telah dirancang ini memiliki banyak kekurangan. Untuk itu ada beberapa saran yang dapat diberikan agar sistem tersebut dapat dikembangkan dan disempurnakan, yaitu:

a. Sistem pengendali dapat digunakan pada berbagai jenis jaringan telepon, baik jaringan telepon pubik maupun jaringan telepon lokal (menggunakan nomor ekstensi).
b. Perancangan perangkat keras dapat lebih dioptimalkan karena pada perangkat keras yang dihasilkan dalam penelitian ini memiliki dimensi 26 cm x 19 cm x 8 cm, sehingga kotak casing yang digunakan berukuran lebih kecil dari kotak casing yang digunakan pada penelitian ini.
c. Umpan balik menggunakan rekaman suara sehingga memudahkan operator untuk mengetahui kondisi sistem. Selain itu dengan adanya rekaman suara,

orang yang tidak tahu adanya sistem pengendali tersebut tidak bingung ketika melakukan panggilan ke nomor telepon yang terhubung dengan sistem pengendali karena rekaman suara dapat memberitahukan kepada penelepon bahwa telepon telah terangkat secara otomatis.

d. Fungsi pengendalian dapat lebih dikembangkan lagi, tidak hanya sebatas pada *ON-OFF* saja. Salah satu pengembangan yang dapat dilakukan adalah dengan mengintegrasikan sistem ini dengan LED *dot matrix* sebagai penampil sehingga dapat tercipta sistem informasi yang cukup efektif.
e. Perancangan tidak hanya sebatas pada perancangan alat saja, namun juga dapat dikembangkan dengan perancangan kemasan produk, uji kehandalan produk, perhitungan yang lebih detail mengenai biaya produksi, serta analisis kebutuhan pasar.

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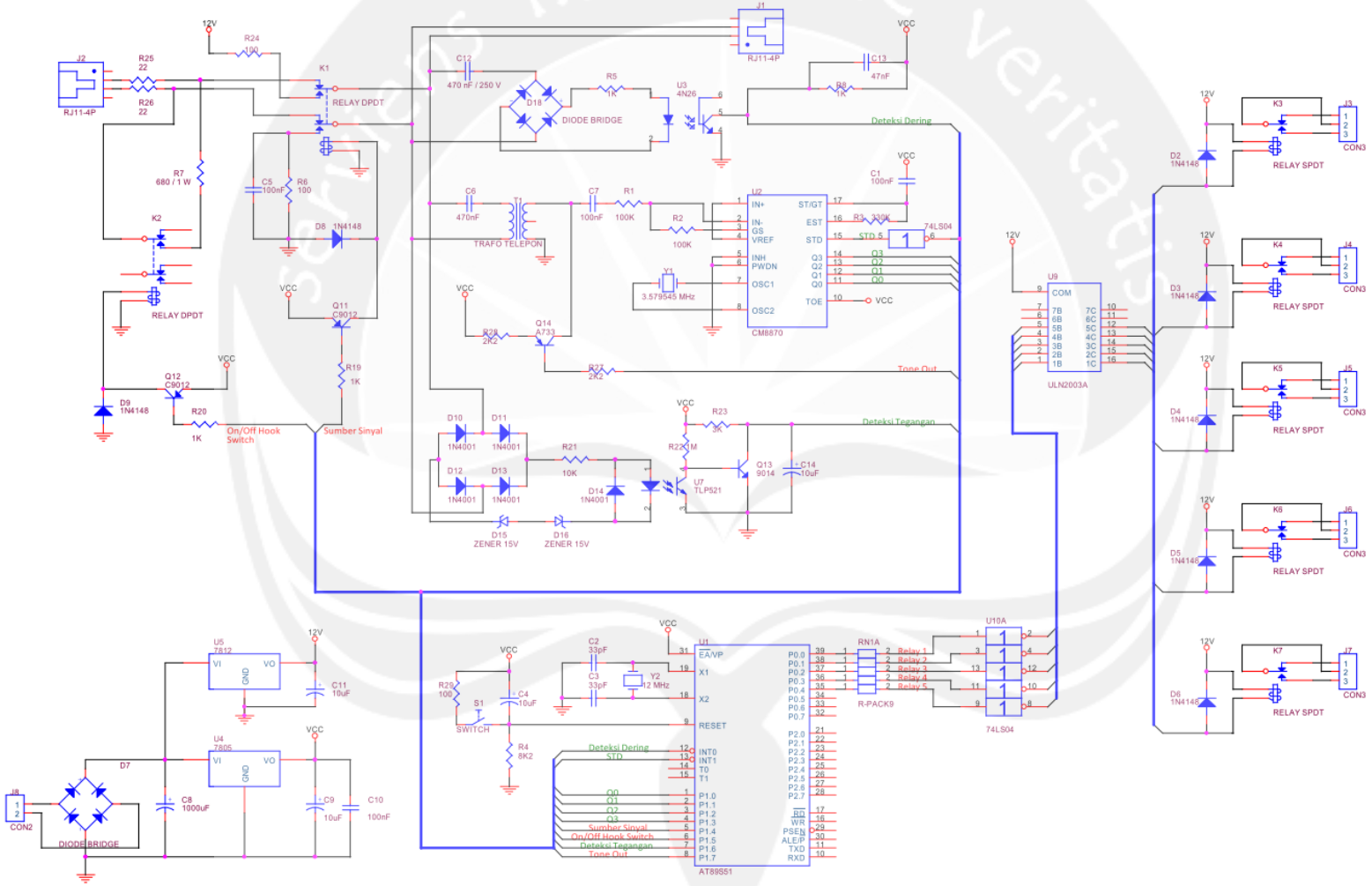
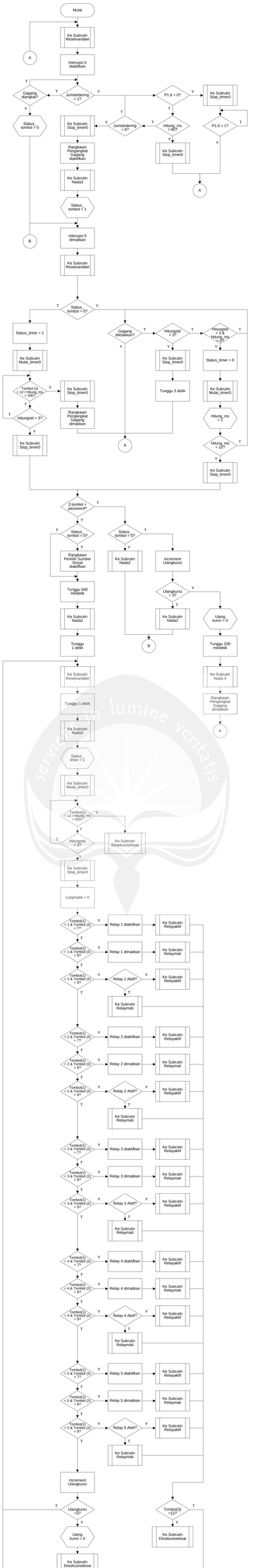
Lampiran 1. Skematik Rangkaian Perangkat Keras



Lampiran 2. Diagram Alir Program Utama



```
$regfile = "Reg51.dat"
$crystal = 12000000

Dim Hitung_ms As Word
Dim Time As Word
Dim Hitungstd As Byte , Tombol(4) As Byte
Dim Dtmf As Byte , Convertdtmf As Byte
Dim Freq As Integer , Count As Integer
Dim Loopnada As Byte , Pengali As Word , Status_timer As Bit
Dim Status_tombol As Bit
Dim Jumlahdering As Byte
Dim Ulangkunci As Byte

Config Timer0 = Timer , Gate = Internal , Mode = 1
Config Timer1 = Timer , Gate = Internal , Mode = 1

Enable Interrupts
On Int0 Hitung_dering
Enable Int1
On Int1 Cek_tombol
Enable Timer0
On Timer0 Hitung_50ms
Enable Timer1
On Timer1 Suara
$large

Mulai:
Gosub Resetvariabel
Enable Int0
Do
   If P1.6 = 0 Then
      Status_tombol = 0
      P2.1 = 0
      Goto Password
   Elseif Jumlahdering = 1 Then
      Do
      If P1.6 = 0 Then
         Gosub Stop_timer0
         Do
         Loop Until P1.6 = 1
         Goto Mulai
      Elseif Hitung_ms > 80 Then
         '80 x 50 ms = 4.000 ms > 4 Detik
         Gosub Stop_timer0
         Goto Mulai
      End If
      Loop Until Jumlahdering = 6
      Gosub Stop_timer0
      P1.5 = 0
      P2.2 = 0
      Status_tombol = 1
      Gosub Nada3
      Goto Password
```

```
   End If
Loop

Password:
Disable Int0
Gosub Resetvariabel
If Status_tombol = 0 Then
   Do
      If P1.6 = 1 Then
         P2.1 = 1
         Goto Mulai
      Elseif Hitungstd = 3 And Hitung_ms = 0 Then
         Status_timer = 0
         Gosub Mulai_timer0
         Hitung_ms = 1
      Elseif Hitungstd > 3 Then
         Do
         Loop Until P1.6 = 1
         Goto Mulai
      End If
   Loop Until Hitung_ms = 10                          ' 0,5 detik
   Gosub Stop_timer0
Elseif Status_tombol = 1 Then
   Status_timer = 1
   Gosub Mulai_timer0
   Do
      If Tombol(1) = 12 Or Hitung_ms = 231 Then       ' 10 detik
         Gosub Stop_timer0
         P1.5 = 1
         Goto Mulai
      End If
   Loop Until Hitungstd = 3
   Gosub Stop_timer0
End If

Cek_password:
If Tombol(1) = 1 And Tombol(2) = 5 And Tombol(3) = 9 Then
   If Status_tombol = 0 Then
      P1.4 = 0
      P2.2 = 0
   End If
   P2.1 = 0
   Waitmse 500
   Gosub Nada1
   Wait 1
   Goto Eksekusi
Else
   If Status_tombol = 0 Then
      Gosub Nada2
      Goto Password
   Elseif Status_tombol = 1 Then
      Incr Ulangkunci
      If Ulangkunci = 3 Then
```

```
107             Ulangkunci = 0
108             Waitms 200
109             Gosub Nada4
110             P1.5 = 1
111             Goto Mulai
112          End If
113          Waitms 250
114          Gosub Nada2
115          Goto Password
116       End If
117    End If
118
119    Eksekusi:
120    Gosub Resetvariabel
121    Wait 1
122    Gosub Nada3
123    Status_timer = 1
124    Gosub Mulai_timer0
125    Do
126       If Tombol(1) = 12 Then
127          Goto Eksekusiselesai
128       Elseif Hitung_ms > 600 Then
129          '600 x 50 ms = 30.000 ms = 30 detik
130          Goto Eksekusiselesai
131       End If
132    Loop Until Hitungstd = 3
133    Gosub Stop_timer0
134
135    'Relay selector
136    'Relay 1
137    If Tombol(1) = 1 And Tombol(2) = 7 Then
138       P0.0 = 0
139       Gosub Relayaktif
140    Elseif Tombol(1) = 1 And Tombol(2) = 8 Then
141       P0.0 = 1
142       Gosub Relaymati
143    Elseif Tombol(1) = 1 And Tombol(2) = 9 Then
144       If P0.0 = 0 Then
145          Gosub Relayaktif
146       Elseif P0.0 = 1 Then
147          Gosub Relaymati
148       End If
149    'Relay 2
150    Elseif Tombol(1) = 2 And Tombol(2) = 7 Then
151       P0.1 = 0
152       Gosub Relayaktif
153    Elseif Tombol(1) = 2 And Tombol(2) = 8 Then
154       P0.1 = 1
155       Gosub Relaymati
156    Elseif Tombol(1) = 2 And Tombol(2) = 9 Then
157       If P0.1 = 0 Then
158          Gosub Relayaktif
159       Elseif P0.1 = 1 Then
```

```
160         Gosub Relaymati
161      End If
162  'Relay 3
163  Elseif Tombol(1) = 3 And Tombol(2) = 7 Then
164      P0.2 = 0
165      Gosub Relayaktif
166  Elseif Tombol(1) = 3 And Tombol(2) = 8 Then
167      P0.2 = 1
168      Gosub Relaymati
169  Elseif Tombol(1) = 3 And Tombol(2) = 9 Then
170      If P0.2 = 0 Then
171          Gosub Relayaktif
172      Elseif P0.2 = 1 Then
173          Gosub Relaymati
174      End If
175  'Relay 4
176  Elseif Tombol(1) = 4 And Tombol(2) = 7 Then
177      P0.3 = 0
178      Gosub Relayaktif
179  Elseif Tombol(1) = 4 And Tombol(2) = 8 Then
180      P0.3 = 1
181      Gosub Relaymati
182  Elseif Tombol(1) = 4 And Tombol(2) = 9 Then
183      If P0.3 = 0 Then
184          Gosub Relayaktif
185      Elseif P0.3 = 1 Then
186          Gosub Relaymati
187      End If
188  'Relay 5
189  Elseif Tombol(1) = 5 And Tombol(2) = 7 Then
190      P0.4 = 0
191      Gosub Relayaktif
192  Elseif Tombol(1) = 5 And Tombol(2) = 8 Then
193      P0.4 = 1
194      Gosub Relaymati
195  Elseif Tombol(1) = 5 And Tombol(2) = 9 Then
196      If P0.4 = 0 Then
197          Gosub Relayaktif
198      Elseif P0.4 = 1 Then
199          Gosub Relaymati
200      End If
201  'Tombol tidak sesuai
202  Else
203      Incr Ulangkunci
204      If Ulangkunci = 3 Then
205          Ulangkunci = 0
206          Goto Eksekusiselesai
207      End If
208      Goto Eksekusi
209  End If
210
211  If Tombol(3) = 12 Then
212      Goto Eksekusiselesai
```

```
213 Else
214    Goto Eksekusi
215 End If
216
217 End
218
219
220 '-------------------------------------------------------------------
221 ' Subrutin Interupsi dan Timer
222 '-------------------------------------------------------------------
223 Resetvariabel:
224    Time = -50000
225    Tombol(1) = 0
226    Tombol(2) = 0
227    Tombol(3) = 0
228    Tombol(4) = 0
229    Jumlahdering = 0
230    Hitungstd = 0
231    Freq = 0
232    Count = 0
233    Loopnada = 0
234    Status_timer = 0
235    Hitung_ms = 0
236 Return
237
238 '-----------------
239 'Interupsi Dering
240 '-----------------
241 Hitung_dering:
242    Wait 2
243    Gosub Stop_timer0
244    Incr Jumlahdering
245    P2.2 = Not P2.2
246    Hitung_ms = 0
247    Status_timer = 0
248    'Status_tombol = 1
249    Gosub Mulai_timer0
250 Return
251
252 '-----------------
253 ' Interupsi Tombol
254 '-----------------
255 Cek_tombol:
256    Incr Hitungstd
257    Dtmf = P1 And &H0F
258       'Port 1 di AND dengan &H0F agar yang terbaca hanya P1.0 - P1.3
259    Convertdtmf = Lookup(dtmf , Dtmf_tabel)
260       'Cek hasil Dtmf dengan Dtmf_tabel
261    Tombol(hitungstd) = Convertdtmf
262    Waitmse 700
263
264    If Status_tombol = 1 Then
265       Count = 501
```

```
266         Gosub 1khz
267      End If
268  Return
269
270      Dtmf_tabel:
271      Data 16 , 1 , 2 , 3 , 4 , 5 , 6 , 7 , 8 , 9 , 10 , 11 , 12 , 13
     , 14 , 15
272           ' D , 1 , 2 , 3 , 4 , 5 , 6 , 7 , 8 , 9 ,  0 ,  * ,  # ,  A
     ,  B ,  C
273           ' 0 , 1 , 2 , 3 , 4 , 5 , 6 , 7 , 8 , 9 , 10 , 11 , 12 , 13
     , 14 , 15
274
275  '-----------------
276  ' Timer 50 mS
277  '-----------------
278  Hitung_50ms:
279      Incr Hitung_ms
280      Reset Tcon.5
281      Gosub Mulai_timer0
282  Return
283
284  Stop_timer0:
285      Stop Timer0
286      Reset Tcon.5
287  Return
288
289  Mulai_timer0:
290      Tl0 = Low(time)
291      Th0 = High(time)
292      Start Timer0
293  Return
294
295  '-----------------
296  'Pengendali Relay
297  '-----------------
298  Relayaktif:
299      Gosub Nadaindikator
300      Wait 1
301      Gosub Nada6
302  Return
303
304  Relaymati:
305      Gosub Nadaindikator
306      Wait 1
307      Gosub Nada7
308  Return
309
310  Eksekusiselesai:
311      Gosub Stop_timer0
312      Wait 2
313      Gosub Nada4
314      P1.4 = 1
315      P1.5 = 1
```

```
316     P2 = 255
317     Goto Mulai
318
319  '-----------------
320  ' Aktivasi Suara
321  '-----------------
322  Suara:
323     Stop Timer1
324     P1.7 = Not P1.7
325     Decr Count
326     Th1 = High(freq)
327     Tl1 = Low(freq)
328     Start Timer1
329     Return
330
331  Lamasuara:
332     Do
333     Loop Until Count = 0
334     Stop Timer1
335  Return
336
337  '-----------------
338  ' Nada indikator
339  '-----------------
340  Nadaindikator:
341     Do
342     Waitms 100
343     Incr Loopnada
344     Gosub Nada5
345     Loop Until Loopnada = Tombol(1)
346     Loopnada = 0
347  Return
348
349  '-----------------
350  ' FREKUENSI SUARA
351  '-----------------
352  500hz:
353     Freq = -1000
354     Gosub Suara
355     Gosub Lamasuara
356  Return
357
358  750hz:
359     Freq = -667
360     Gosub Suara
361     Gosub Lamasuara
362  Return
363
364  1khz:
365     Freq = -500
366     Gosub Suara
367     Gosub Lamasuara
368  Return
```

```
369
370 1.25khz:
371    Freq = -400
372    Gosub Suara
373    Gosub Lamasuara
374 Return
375
376 1.5khz:
377    Freq = -333
378    Gosub Suara
379    Gosub Lamasuara
380 Return
381
382 1.75khz:
383    Freq = -286
384    Gosub Suara
385    Gosub Lamasuara
386 Return
387
388 '-----------------
389 ' Tone Generator
390 '-----------------
391 Nada1:
392    Do
393    Incr Loopnada
394    Count = 126
395    Gosub 500hz
396    Count = 188
397    Gosub 750hz
398    Count = 251
399    Gosub 1khz
400    Count = 313
401    Loop Until Loopnada = 2
402    Loopnada = 0
403 Return
404
405 Nada2:
406    Do
407    Incr Loopnada
408    Count = 251
409    Gosub 1khz
410    Count = 188
411    Gosub 750hz
412    Count = 126
413    Gosub 500hz
414    Loop Until Loopnada = 2
415    Loopnada = 0
416 Return
417
418 Nada3:
419    Count = 126
420    Gosub 500hz
421    Count = 188
```

```
422     Gosub 750hz
423     Count = 251
424     Gosub 1khz
425     Waitms 250
426     Count = 251
427     Gosub 1khz
428     Count = 188
429     Gosub 750hz
430     Count = 126
431     Gosub 500hz
432 Return
433
434 Nada4:
435     Do
436     Incr Loopnada
437     Count = 751
438     Gosub 750hz
439     Waitmse 400
440     Loop Until Loopnada = 3
441     Loopnada = 0
442 Return
443
444 Nada5:
445     Count = 751
446     Gosub 1khz
447     Waitmse 500
448 Return
449
450 Nada6:
451     Count = 126
452     Gosub 500hz
453     Count = 188
454     Gosub 750hz
455     Count = 251
456     Gosub 1khz
457     Count = 313
458     Gosub 1.25khz
459     Count = 376
460     Gosub 1.5khz
461     Count = 438
462     Gosub 1.75khz
463 Return
464
465 Nada7:
466     Count = 438
467     Gosub 1.75khz
468     Count = 376
469     Gosub 1.5khz
470     Count = 313
471     Gosub 1.25khz
472     Count = 251
473     Gosub 1khz
474     Count = 188
```

```
    Gosub 750hz
    Count = 126
    Gosub 500hz
Return
```

Lampiran 4. Tabel Uji Coba Alat

Tabel Uji Coba Sistem Pengendalian Secara Global

Uji Coba 1 - Pengendali Melakukan Pengendalian Secara Berulang-Ulang

No	Urutan Proses Uji Coba	Percobaan				
		1	2	3	4	5
1	Melakukan panggilan (6 kali dering)	√	√	√	√	√
2	Sambungan telepon terhubung	√	√	√	√	√
3	Muncul Nada 3	√	√	√	√	√
4	Memasukkan password dengan benar	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
5	Muncul Nada 1	√	√	√	√	√
6	Muncul Nada 3	√	√	√	√	√
7	Mengaktifkan beban pertama (1-7-0)	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
8	Muncul Nada indikator 1 kali	√	√	√	√	√
9	Muncul Nada 6	√	√	√	√	√
10	Muncul Nada 3	√	√	√	√	√
11	Menanyakan status beban pertama (1-9-0)	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
12	Muncul Nada indikator 1 kali	√	√	√	√	√
13	Muncul Nada 6	√	√	√	√	√

14	Muncul Nada 3	√	√	√	√	√
15	Menonaktifkan beban pertama (1-8-0)	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
16	Muncul Nada indikator 1 kali	√	√	√	√	√
17	Muncul Nada 7	√	√	√	√	√
18	Muncul Nada 3	√	√	√	√	√
19	Menanyakan status beban pertama (1-9-0)	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
20	Muncul Nada indikator 1 kali	√	√	√	√	√
21	Muncul Nada 7	√	√	√	√	√
22	Muncul Nada 3	√	√	√	√	√
23	Mengaktifkan beban kedua (2-7-0)	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
24	Muncul Nada indikator 2 kali	√	√	√	√	√
25	Muncul Nada 6	√	√	√	√	√
26	Muncul Nada 3	√	√	√	√	√
27	Menanyakan status beban kedua (2-9-0)	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
28	Muncul Nada indikator 2 kali	√	√	√	√	√
29	Muncul Nada 6	√	√	√	√	√
30	Muncul Nada 3	√	√	√	√	√
31	Menonaktifkan beban kedua (2-8-0)	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
32	Muncul Nada indikator 2 kali	√	√	√	√	√

33	Muncul Nada 7	√	√	√	√	√
34	Muncul Nada 3	√	√	√	√	√
35	Menanyakan status beban kedua (2-9-0)	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
36	Muncul Nada indikator 2 kali	√	√	√	√	√
37	Muncul Nada 7	√	√	√	√	√
38	Muncul Nada 3	√	√	√	√	√
39	Mengaktifkan beban ketiga (3-7-0)	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
40	Muncul Nada indikator 3 kali	√	√	√	√	√
41	Muncul Nada 6	√	√	√	√	√
42	Muncul Nada 3	√	√	√	√	√
43	Menanyakan status beban ketiga (3-9-0)	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
44	Muncul Nada indikator 3 kali	√	√	√	√	√
45	Muncul Nada 6	√	√	√	√	√
46	Muncul Nada 3	√	√	√	√	√
47	Menonaktifkan beban ketiga (3-8-0)	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
48	Muncul Nada indikator 3 kali	√	√	√	√	√
49	Muncul Nada 7	√	√	√	√	√
50	Muncul Nada 3	√	√	√	√	√
51	Menanyakan status beban ketiga (3-9-0)	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√

52	Muncul Nada indikator 3 kali	√	√	√	√	√
53	Muncul Nada 7	√	√	√	√	√
54	Muncul Nada 3	√	√	√	√	√
55	Mengaktifkan beban keempat (4-7-0)	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
56	Muncul Nada indikator 4 kali	√	√	√	√	√
57	Muncul Nada 6	√	√	√	√	√
58	Muncul Nada 3	√	√	√	√	√
59	Menanyakan status beban keempat (4-9-0)	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
60	Muncul Nada indikator 4 kali	√	√	√	√	√
61	Muncul Nada 6	√	√	√	√	√
62	Muncul Nada 3	√	√	√	√	√
63	Menonaktifkan beban keempat (4-8-0)	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
64	Muncul Nada indikator 4 kali	√	√	√	√	√
65	Muncul Nada 7	√	√	√	√	√
66	Muncul Nada 3	√	√	√	√	√
67	Menanyakan status beban keempat (4-9-0)	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
68	Muncul Nada indikator 4 kali	√	√	√	√	√
69	Muncul Nada 7	√	√	√	√	√
70	Muncul Nada 3	√	√	√	√	√
71	Mengaktifkan beban kelima (5-7-0)	√	√	√	√	√

	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
72	Muncul Nada indikator 5 kali	√	√	√	√	√
73	Muncul Nada 6	√	√	√	√	√
74	Muncul Nada 3	√	√	√	√	√
75	Menanyakan status beban kelima (5-9-0)	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
76	Muncul Nada indikator 5 kali	√	√	√	√	√
77	Muncul Nada 6	√	√	√	√	√
78	Muncul Nada 3	√	√	√	√	√
79	Menonaktifkan beban kelima (5-8-0)	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
80	Muncul Nada indikator 5 kali	√	√	√	√	√
81	Muncul Nada 7	√	√	√	√	√
82	Muncul Nada 3	√	√	√	√	√
83	Menanyakan status beban kelima (5-9-0)	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
84	Muncul Nada indikator 5 kali	√	√	√	√	√
85	Muncul Nada 7	√	√	√	√	√
86	Muncul Nada 3	√	√	√	√	√

Tabel Uji Coba Sistem Pengendalian Secara Global

Uji Coba 2 Bagian Pertama – Pengendali Mengaktifkan Beban Dan Selesai Memberikan Perintah

a. Beban Pertama

No	Urutan Proses Uji Coba	Percobaan				
		1	2	3	4	5
1	Melakukan panggilan (6 kali dering)	√	√	√	√	√
2	Sambungan telepon terhubung	√	√	√	√	√
3	Muncul Nada 3	√	√	√	√	√
4	Memasukkan password dengan benar	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
5	Muncul Nada 1	√	√	√	√	√
6	Muncul Nada 3	√	√	√	√	√
7	Memasukkan kode perintah (1-7-#)	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
8	Muncul Nada indikator 1 kali	√	√	√	√	√
9	Muncul Nada 6	√	√	√	√	√
10	Muncul Nada 4	√	√	√	√	√
11	Sambungan telepon terputus	√	√	√	√	√

b. Beban Kedua

No	Urutan Proses Uji Coba	Percobaan				
		1	2	3	4	5
1	Melakukan panggilan (6 kali dering)	√	√	√	√	√
2	Sambungan telepon terhubung	√	√	√	√	√
3	Muncul Nada 3	√	√	√	√	√
4	Memasukkan password dengan benar	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
5	Muncul Nada 1	√	√	√	√	√
6	Muncul Nada 3	√	√	√	√	√
7	Memasukkan kode perintah (2-7-#)	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
8	Muncul Nada indikator 2 kali	√	√	√	√	√
9	Muncul Nada 6	√	√	√	√	√
10	Muncul Nada 4	√	√	√	√	√
11	Sambungan telepon terputus	√	√	√	√	√

c. Beban Ketiga

No	Urutan Proses Uji Coba	Percobaan				
		1	2	3	4	5
1	Melakukan panggilan (6 kali dering)	√	√	√	√	√
2	Sambungan telepon terhubung	√	√	√	√	√
3	Muncul Nada 3	√	√	√	√	√

4	Memasukkan password dengan benar	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
5	Muncul Nada 1	√	√	√	√	√
6	Muncul Nada 3	√	√	√	√	√
7	Memasukkan kode perintah (3-7-#)	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
8	Muncul Nada indikator 3 kali	√	√	√	√	√
9	Muncul Nada 6	√	√	√	√	√
10	Muncul Nada 4	√	√	√	√	√
11	Sambungan telepon terputus	√	√	√	√	√

d. Beban Keempat

No	**Urutan Proses Uji Coba**	**Percobaan**				
		1	**2**	**3**	**4**	**5**
1	Melakukan panggilan (6 kali dering)	√	√	√	√	√
2	Sambungan telepon terhubung	√	√	√	√	√
3	Muncul Nada 3	√	√	√	√	√
4	Memasukkan password dengan benar	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
5	Muncul Nada 1	√	√	√	√	√
6	Muncul Nada 3	√	√	√	√	√
7	Memasukkan kode perintah (4-7-#)	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√

8	Muncul Nada indikator 4 kali	√	√	√	√	√
9	Muncul Nada 6	√	√	√	√	√
10	Muncul Nada 4	√	√	√	√	√
11	Sambungan telepon terputus	√	√	√	√	√

e. Beban Kelima

No	Urutan Proses Uji Coba	Percobaan				
		1	2	3	4	5
1	Melakukan panggilan (6 kali dering)	√	√	√	√	√
2	Sambungan telepon terhubung	√	√	√	√	√
3	Muncul Nada 3	√	√	√	√	√
4	Memasukkan password dengan benar	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
5	Muncul Nada 1	√	√	√	√	√
6	Muncul Nada 3	√	√	√	√	√
7	Memasukkan kode perintah (5-7-#)	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
8	Muncul Nada indikator 5 kali	√	√	√	√	√
9	Muncul Nada 6	√	√	√	√	√
10	Muncul Nada 4	√	√	√	√	√
11	Sambungan telepon terputus	√	√	√	√	√

Tabel Uji Coba Sistem Pengendalian Secara Global

Uji Coba 2 Bagian Kedua - Pengendali Menanyakan Status Beban (Dalam Kondisi Aktif) Dan Selesai Memberikan Perintah

a. Beban Pertama

No	Urutan Proses Uji Coba	Percobaan				
		1	2	3	4	5
1	Melakukan panggilan (6 kali dering)	√	√	√	√	√
2	Sambungan telepon terhubung	√	√	√	√	√
3	Muncul Nada 3	√	√	√	√	√
4	Memasukkan password dengan benar	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
5	Muncul Nada 1	√	√	√	√	√
6	Muncul Nada 3	√	√	√	√	√
7	Memasukkan kode perintah (1-9-#)	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
8	Muncul Nada indikator 1 kali	√	√	√	√	√
9	Muncul Nada 6	√	√	√	√	√
10	Muncul Nada 4	√	√	√	√	√
11	Sambungan telepon terputus	√	√	√	√	√

b. Beban Kedua

No	Urutan Proses Uji Coba	Percobaan				
		1	2	3	4	5
1	Melakukan panggilan (6 kali dering)	√	√	√	√	√
2	Sambungan telepon terhubung	√	√	√	√	√
3	Muncul Nada 3	√	√	√	√	√
4	Memasukkan password dengan benar	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
5	Muncul Nada 1	√	√	√	√	√
6	Muncul Nada 3	√	√	√	√	√
7	Memasukkan kode perintah (2-9-#)	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
8	Muncul Nada indikator 2 kali	√	√	√	√	√
9	Muncul Nada 6	√	√	√	√	√
10	Muncul Nada 4	√	√	√	√	√
11	Sambungan telepon terputus	√	√	√	√	√

c. Beban Ketiga

No	Urutan Proses Uji Coba	Percobaan				
		1	2	3	4	5
1	Melakukan panggilan (6 kali dering)	√	√	√	√	√
2	Sambungan telepon terhubung	√	√	√	√	√
3	Muncul Nada 3	√	√	√	√	√

4	Memasukkan password dengan benar	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
5	Muncul Nada 1	√	√	√	√	√
6	Muncul Nada 3	√	√	√	√	√
7	Memasukkan kode perintah (3-9-#)	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
8	Muncul Nada indikator 3 kali	√	√	√	√	√
9	Muncul Nada 6	√	√	√	√	√
10	Muncul Nada 4	√	√	√	√	√
11	Sambungan telepon terputus	√	√	√	√	√

d. Beban Keempat

No	**Urutan Proses Uji Coba**	**Percobaan**				
		1	**2**	**3**	**4**	**5**
1	Melakukan panggilan (6 kali dering)	√	√	√	√	√
2	Sambungan telepon terhubung	√	√	√	√	√
3	Muncul Nada 3	√	√	√	√	√
4	Memasukkan password dengan benar	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
5	Muncul Nada 1	√	√	√	√	√
6	Muncul Nada 3	√	√	√	√	√
7	Memasukkan kode perintah (4-9-#)	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√

8	Muncul Nada indikator 4 kali	√	√	√	√	√
9	Muncul Nada 6	√	√	√	√	√
10	Muncul Nada 4	√	√	√	√	√
11	Sambungan telepon terputus	√	√	√	√	√

e. Beban Kelima

No	Urutan Proses Uji Coba	Percobaan				
		1	2	3	4	5
1	Melakukan panggilan (6 kali dering)	√	√	√	√	√
2	Sambungan telepon terhubung	√	√	√	√	√
3	Muncul Nada 3	√	√	√	√	√
4	Memasukkan password dengan benar	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
5	Muncul Nada 1	√	√	√	√	√
6	Muncul Nada 3	√	√	√	√	√
7	Memasukkan kode perintah (5-9-#)	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
8	Muncul Nada indikator 5 kali	√	√	√	√	√
9	Muncul Nada 6	√	√	√	√	√
10	Muncul Nada 4	√	√	√	√	√
11	Sambungan telepon terputus	√	√	√	√	√

Tabel Uji Coba Sistem Pengendalian Secara Global

Uji Coba 2 Bagian Ketiga - Pengendali Menonaktifkan Beban Dan Selesai Memberikan Perintah

a. Beban Pertama

No	Urutan Proses Uji Coba	Percobaan				
		1	2	3	4	5
1	Melakukan panggilan (6 kali dering)	√	√	√	√	√
2	Sambungan telepon terhubung	√	√	√	√	√
3	Muncul Nada 3	√	√	√	√	√
4	Memasukkan password dengan benar	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
5	Muncul Nada 1	√	√	√	√	√
6	Muncul Nada 3	√	√	√	√	√
7	Memasukkan kode perintah (1-8-#)	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
8	Muncul Nada indikator 1 kali	√	√	√	√	√
9	Muncul Nada 7	√	√	√	√	√
10	Muncul Nada 4	√	√	√	√	√
11	Sambungan telepon terputus	√	√	√	√	√

b. Beban Kedua

No	Urutan Proses Uji Coba	Percobaan				
		1	2	3	4	5
1	Melakukan panggilan (6 kali dering)	√	√	√	√	√
2	Sambungan telepon terhubung	√	√	√	√	√
3	Muncul Nada 3	√	√	√	√	√
4	Memasukkan password dengan benar	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
5	Muncul Nada 1	√	√	√	√	√
6	Muncul Nada 3	√	√	√	√	√
7	Memasukkan kode perintah (2-8-#)	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
8	Muncul Nada indikator 2 kali	√	√	√	√	√
9	Muncul Nada 7	√	√	√	√	√
10	Muncul Nada 4	√	√	√	√	√
11	Sambungan telepon terputus	√	√	√	√	√

c. Beban Ketiga

No	Urutan Proses Uji Coba	Percobaan				
		1	2	3	4	5
1	Melakukan panggilan (6 kali dering)	√	√	√	√	√
2	Sambungan telepon terhubung	√	√	√	√	√
3	Muncul Nada 3	√	√	√	√	√

4	Memasukkan password dengan benar	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
5	Muncul Nada 1	√	√	√	√	√
6	Muncul Nada 3	√	√	√	√	√
7	Memasukkan kode perintah (3-8-#)	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
8	Muncul Nada indikator 3 kali	√	√	√	√	√
9	Muncul Nada 7	√	√	√	√	√
10	Muncul Nada 4	√	√	√	√	√
11	Sambungan telepon terputus	√	√	√	√	√

d. Beban Keempat

No	**Urutan Proses Uji Coba**	**Percobaan**				
		1	**2**	**3**	**4**	**5**
1	Melakukan panggilan (6 kali dering)	√	√	√	√	√
2	Sambungan telepon terhubung	√	√	√	√	√
3	Muncul Nada 3	√	√	√	√	√
4	Memasukkan password dengan benar	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
5	Muncul Nada 1	√	√	√	√	√
6	Muncul Nada 3	√	√	√	√	√
7	Memasukkan kode perintah (4-8-#)	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√

8	Muncul Nada indikator 4 kali	√	√	√	√	√
9	Muncul Nada 7	√	√	√	√	√
10	Muncul Nada 4	√	√	√	√	√
11	Sambungan telepon terputus	√	√	√	√	√

e. Beban Kelima

No	Urutan Proses Uji Coba	Percobaan				
		1	2	3	4	5
1	Melakukan panggilan (6 kali dering)	√	√	√	√	√
2	Sambungan telepon terhubung	√	√	√	√	√
3	Muncul Nada 3	√	√	√	√	√
4	Memasukkan password dengan benar	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
5	Muncul Nada 1	√	√	√	√	√
6	Muncul Nada 3	√	√	√	√	√
7	Memasukkan kode perintah (5-8-#)	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
8	Muncul Nada indikator 5 kali	√	√	√	√	√
9	Muncul Nada 7	√	√	√	√	√
10	Muncul Nada 4	√	√	√	√	√
11	Sambungan telepon terputus	√	√	√	√	√

Tabel Uji Coba Sistem Pengendalian Secara Global

Uji Coba 2 Bagian Keempat - Pengendali Menanyakan Status Beban (Dalam Kondisi Nonaktif) Dan Selesai Memberikan Perintah

a. Beban Pertama

No	Urutan Proses Uji Coba	Percobaan				
		1	2	3	4	5
1	Melakukan panggilan (6 kali dering)	√	√	√	√	√
2	Sambungan telepon terhubung	√	√	√	√	√
3	Muncul Nada 3	√	√	√	√	√
4	Memasukkan password dengan benar	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
5	Muncul Nada 1	√	√	√	√	√
6	Muncul Nada 3	√	√	√	√	√
7	Memasukkan kode perintah (1-9-#)	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
8	Muncul Nada indikator 1 kali	√	√	√	√	√
9	Muncul Nada 7	√	√	√	√	√
10	Muncul Nada 4	√	√	√	√	√
11	Sambungan telepon terputus	√	√	√	√	√

b. Beban Kedua

No	Urutan Proses Uji Coba	Percobaan				
		1	2	3	4	5
1	Melakukan panggilan (6 kali dering)	√	√	√	√	√
2	Sambungan telepon terhubung	√	√	√	√	√
3	Muncul Nada 3	√	√	√	√	√
4	Memasukkan password dengan benar	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
5	Muncul Nada 1	√	√	√	√	√
6	Muncul Nada 3	√	√	√	√	√
7	Memasukkan kode perintah (2-9-#)	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
8	Muncul Nada indikator 2 kali	√	√	√	√	√
9	Muncul Nada 7	√	√	√	√	√
10	Muncul Nada 4	√	√	√	√	√
11	Sambungan telepon terputus	√	√	√	√	√

c. Beban Ketiga

No	Urutan Proses Uji Coba	Percobaan				
		1	2	3	4	5
1	Melakukan panggilan (6 kali dering)	√	√	√	√	√
2	Sambungan telepon terhubung	√	√	√	√	√
3	Muncul Nada 3	√	√	√	√	√

4	Memasukkan password dengan benar	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
5	Muncul Nada 1	√	√	√	√	√
6	Muncul Nada 3	√	√	√	√	√
7	Memasukkan kode perintah (3-9-#)	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
8	Muncul Nada indikator 3 kali	√	√	√	√	√
9	Muncul Nada 7	√	√	√	√	√
10	Muncul Nada 4	√	√	√	√	√
11	Sambungan telepon terputus	√	√	√	√	√

d. Beban Keempat

No	**Urutan Proses Uji Coba**	**Percobaan**				
		1	**2**	**3**	**4**	**5**
1	Melakukan panggilan (6 kali dering)	√	√	√	√	√
2	Sambungan telepon terhubung	√	√	√	√	√
3	Muncul Nada 3	√	√	√	√	√
4	Memasukkan password dengan benar	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
5	Muncul Nada 1	√	√	√	√	√
6	Muncul Nada 3	√	√	√	√	√
7	Memasukkan kode perintah (4-9-#)	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√

8	Muncul Nada indikator 4 kali	√	√	√	√	√
9	Muncul Nada 7	√	√	√	√	√
10	Muncul Nada 4	√	√	√	√	√
11	Sambungan telepon terputus	√	√	√	√	√

e. Beban Kelima

No	Urutan Proses Uji Coba	Percobaan				
		1	2	3	4	5
1	Melakukan panggilan (6 kali dering)	√	√	√	√	√
2	Sambungan telepon terhubung	√	√	√	√	√
3	Muncul Nada 3	√	√	√	√	√
4	Memasukkan password dengan benar	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
5	Muncul Nada 1	√	√	√	√	√
6	Muncul Nada 3	√	√	√	√	√
7	Memasukkan kode perintah (5-9-#)	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
8	Muncul Nada indikator 5 kali	√	√	√	√	√
9	Muncul Nada 7	√	√	√	√	√
10	Muncul Nada 4	√	√	√	√	√
11	Sambungan telepon terputus	√	√	√	√	√

Tabel Uji Coba Sistem Pengendalian Secara Global

Uji Coba 3 – Pengendali Salah Dalam Memasukkan Kode Perintah Sebanyak 3 Kali

No	Urutan Proses Uji Coba	Percobaan				
		1	2	3	4	5
1	Melakukan panggilan (6 kali dering)	√	√	√	√	√
2	Sambungan telepon terhubung	√	√	√	√	√
3	Muncul Nada 3	√	√	√	√	√
4	Memasukkan password dengan benar	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
5	Muncul Nada 1	√	√	√	√	√
6	Muncul Nada 3	√	√	√	√	√
7	Memasukkan kode perintah (pertama)	1-9-7	2-0-7	8-3-#	9-4-#	5-0-7
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
8	Muncul Nada 3	√	√	√	√	√
9	Memasukkan kode perintah (kedua)	9-1-7	7-0-2	3-#-8	9-#-4	8-5-#
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
10	Muncul Nada 3	√	√	√	√	√
11	Memasukkan kode perintah (ketiga)	7-1-9	0-2-7	8-#-3	4-#-9	0-9-5
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
12	Muncul Nada 4	√	√	√	√	√
13	Sambungan telepon terputus	√	√	√	√	√

Tabel Uji Coba Sistem Pengendalian Secara Global

Uji Coba 4 - Pengendali Tidak Memasukkan Kode Perintah Selama 30 Detik

No	Urutan Proses Uji Coba	Percobaan				
		1	2	3	4	5
1	Melakukan panggilan (6 kali dering)	√	√	√	√	√
2	Sambungan telepon terhubung	√	√	√	√	√
3	Muncul Nada 3	√	√	√	√	√
4	Memasukkan password dengan benar	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
5	Muncul Nada 1	√	√	√	√	√
6	Muncul Nada 3	√	√	√	√	√
7	Tidak menekan tombol apapun selama 30 detik	√	√	√	√	√
8	Muncul Nada 4	√	√	√	√	√
9	Sambungan telepon terputus	√	√	√	√	√

Tabel Uji Coba Sistem Pengendalian Secara Global

Uji Coba 5 - Pengendali Menekan Tombol # Sebagai Tombol Pertama Dalam Memasukkan Kode Perintah

No	Urutan Proses Uji Coba	Percobaan				
		1	2	3	4	5
1	Melakukan panggilan (6 kali dering)	√	√	√	√	√
2	Sambungan telepon terhubung	√	√	√	√	√
3	Muncul Nada 3	√	√	√	√	√
4	Memasukkan password dengan benar	√	√	√	√	√
	(Muncul nada tanggapan setiap penekanan tombol)	√	√	√	√	√
5	Muncul Nada 1	√	√	√	√	√
6	Muncul Nada 3	√	√	√	√	√
7	Menekan tombol # sebanyak 1 kali	√	√	√	√	√
8	Muncul Nada 4	√	√	√	√	√
9	Sambungan telepon terputus	√	√	√	√	√

Tabel Uji Coba Sistem Pengendalian Secara Global

Uji Coba 6 - Pengendali Salah Dalam Memasukkan Password Sebanyak 3 Kali

No	Urutan Proses Uji Coba	Percobaan				
		1	2	3	4	5
1	Melakukan panggilan (6 kali dering)	√	√	√	√	√
2	Sambungan telepon terhubung	√	√	√	√	√
3	Muncul Nada 3	√	√	√	√	√
4	Memasukkan password (pertama) (Muncul nada tanggapan setiap penekanan tombol)	9-5-1 √	2-9-5 √	1-2-3 √	1-4-7 √	1-7-9 √
5	Muncul Nada 2	√	√	√	√	√
6	Memasukkan password (kedua) (Muncul nada tanggapan setiap penekanan tombol)	1-9-5 √	2-5-8 √	4-5-6 √	2-5-8 √	1-7-0 √
7	Muncul Nada 2	√	√	√	√	√
8	Memasukkan password (ketiga) (Muncul nada tanggapan setiap penekanan tombol)	5-1-9 √	3-5-7 √	3-6-9 √	7-8-9 √	1-9-# √
9	Muncul Nada 4	√	√	√	√	√
10	Sambungan telepon terputus	√	√	√	√	√

Tabel Uji Coba Sistem Pengendalian Secara Global

Uji Coba 7 - Pengendali Tidak Memasukkan Password Selama 10 Detik

No	Urutan Proses Uji Coba	Percobaan				
		1	2	3	4	5
1	Melakukan panggilan (6 kali dering)	√	√	√	√	√
2	Sambungan telepon terhubung	√	√	√	√	√
3	Muncul Nada 3	√	√	√	√	√
4	Tidak menekan tombol apapun selama 10 detik	√	√	√	√	√
5	Sambungan telepon terputus	√	√	√	√	√

Uji Coba 8 - Pengendali Menekan Tombol # Sebagai Tombol Pertama Dalam Memasukkan Password

No	Urutan Proses Uji Coba	Percobaan				
		1	2	3	4	5
1	Melakukan panggilan (6 kali dering)	√	√	√	√	√
2	Sambungan telepon terhubung	√	√	√	√	√
3	Muncul Nada 3	√	√	√	√	√
4	Menekan tombol # sebanyak 1 kali	√	√	√	√	√
5	Sambungan telepon terputus	√	√	√	√	√

Tabel Uji Coba Sistem Pengendalian Secara Global

Uji Coba 9 - Pengendali Melakukan Panggilan Tidak Terjawab (*Misscall*)

No	Urutan Proses Uji Coba	Percobaan				
		1	2	3	4	5
1	Melakukan panggilan	√	√	√	√	√
2	Panggilan dimatikan (6 kali dering)	√	√	√	√	√
3	Sistem tidak bekerja	√	√	√	√	√

Ujicoba 10 - Panggilan Telepon Dijawab Sebelum 6 Kali Dering

No	Urutan Proses Uji Coba	Percobaan				
		1	2	3	4	5
1	Melakukan panggilan	√	√	√	√	√
2	Panggilan telepon diangkat (< 6 kali dering)	√	√	√	√	√
3	Telepon terhubung	√	√	√	√	√
4	Sistem tidak bekerja	√	√	√	√	√
5	Sambungan telepon dimatikan / Gagang diletakkan	√	√	√	√	√
6	Sistem kembali bekerja	√	√	√	√	√

Tabel Uji Coba Sistem Pengendalian Secara Lokal

Uji Coba 1 - Pengendali Melakukan Pengendalian Secara Berulang-Ulang

No	Urutan Proses Uji Coba	Percobaan				
		1	2	3	4	5
1	Gagang telepon diangkat	√	√	√	√	√
2	Memasukkan password dengan benar	√	√	√	√	√
3	Sinyal berpindah ke tegangan 12 volt DC	√	√	√	√	√
4	Muncul Nada 1	√	√	√	√	√
5	Muncul Nada 3	√	√	√	√	√
6	Mengaktifkan beban pertama (1-7-0)	√	√	√	√	√
7	Muncul Nada indikator 1 kali	√	√	√	√	√
8	Muncul Nada 6	√	√	√	√	√
9	Muncul Nada 3	√	√	√	√	√
10	Menanyakan status beban pertama (1-9-0)	√	√	√	√	√
11	Muncul Nada indikator 1 kali	√	√	√	√	√
12	Muncul Nada 6	√	√	√	√	√
13	Muncul Nada 3	√	√	√	√	√
14	Menonaktifkan beban pertama (1-8-0)	√	√	√	√	√
15	Muncul Nada indikator 1 kali	√	√	√	√	√
16	Muncul Nada 7	√	√	√	√	√
17	Muncul Nada 3	√	√	√	√	√
18	Menanyakan status beban pertama (1-9-0)	√	√	√	√	√

19	Muncul Nada indikator 1 kali	√	√	√	√	√
20	Muncul Nada 7	√	√	√	√	√
21	Muncul Nada 3	√	√	√	√	√
22	Mengaktifkan beban kedua (2-7-0)	√	√	√	√	√
23	Muncul Nada indikator 2 kali	√	√	√	√	√
24	Muncul Nada 6	√	√	√	√	√
25	Muncul Nada 3	√	√	√	√	√
26	Menanyakan status beban kedua (2-9-0)	√	√	√	√	√
27	Muncul Nada indikator 2 kali	√	√	√	√	√
28	Muncul Nada 6	√	√	√	√	√
29	Muncul Nada 3	√	√	√	√	√
30	Menonaktifkan beban kedua (2-8-0)	√	√	√	√	√
31	Muncul Nada indikator 2 kali	√	√	√	√	√
32	Muncul Nada 7	√	√	√	√	√
33	Muncul Nada 3	√	√	√	√	√
34	Menanyakan status beban kedua (2-9-0)	√	√	√	√	√
35	Muncul Nada indikator 2 kali	√	√	√	√	√
36	Muncul Nada 7	√	√	√	√	√
37	Muncul Nada 3	√	√	√	√	√
38	Mengaktifkan beban ketiga (3-7-0)	√	√	√	√	√
39	Muncul Nada indikator 3 kali	√	√	√	√	√
40	Muncul Nada 6	√	√	√	√	√
41	Muncul Nada 3	√	√	√	√	√
42	Menanyakan status beban ketiga (3-9-0)	√	√	√	√	√

43	Muncul Nada indikator 3 kali	√	√	√	√	√
44	Muncul Nada 6	√	√	√	√	√
45	Muncul Nada 3	√	√	√	√	√
46	Menonaktifkan beban ketiga (3-8-0)	√	√	√	√	√
47	Muncul Nada indikator 3 kali	√	√	√	√	√
48	Muncul Nada 7	√	√	√	√	√
49	Muncul Nada 3	√	√	√	√	√
50	Menanyakan status beban ketiga (3-9-0)	√	√	√	√	√
51	Muncul Nada indikator 3 kali	√	√	√	√	√
52	Muncul Nada 7	√	√	√	√	√
53	Muncul Nada 3	√	√	√	√	√
54	Mengaktifkan beban keempat (4-7-0)	√	√	√	√	√
55	Muncul Nada indikator 4 kali	√	√	√	√	√
56	Muncul Nada 6	√	√	√	√	√
57	Muncul Nada 3	√	√	√	√	√
58	Menanyakan status beban keempat (4-9-0)	√	√	√	√	√
59	Muncul Nada indikator 4 kali	√	√	√	√	√
60	Muncul Nada 6	√	√	√	√	√
61	Muncul Nada 3	√	√	√	√	√
62	Menonaktifkan beban keempat (4-8-0)	√	√	√	√	√
63	Muncul Nada indikator 4 kali	√	√	√	√	√
64	Muncul Nada 7	√	√	√	√	√
65	Muncul Nada 3	√	√	√	√	√
66	Menanyakan status beban keempat (4-9-0)	√	√	√	√	√

67	Muncul Nada indikator 4 kali	√	√	√	√	√
68	Muncul Nada 7	√	√	√	√	√
69	Muncul Nada 3	√	√	√	√	√
70	Mengaktifkan beban kelima (5-7-0)	√	√	√	√	√
71	Muncul Nada indikator 5 kali	√	√	√	√	√
72	Muncul Nada 6	√	√	√	√	√
73	Muncul Nada 3	√	√	√	√	√
74	Menanyakan status beban kelima (5-9-0)	√	√	√	√	√
75	Muncul Nada indikator 5 kali	√	√	√	√	√
76	Muncul Nada 6	√	√	√	√	√
77	Muncul Nada 3	√	√	√	√	√
78	Menonaktifkan beban kelima (5-8-0)	√	√	√	√	√
79	Muncul Nada indikator 5 kali	√	√	√	√	√
80	Muncul Nada 7	√	√	√	√	√
81	Muncul Nada 3	√	√	√	√	√
82	Menanyakan status beban kelima (5-9-0)	√	√	√	√	√
83	Muncul Nada indikator 5 kali	√	√	√	√	√
84	Muncul Nada 7	√	√	√	√	√
85	Muncul Nada 3	√	√	√	√	√

Tabel Uji Coba Sistem Pengendalian Secara Lokal

Uji Coba 2 Bagian Pertama - Pengendali Mengaktifkan Beban Dan Selesai Memberikan Perintah

a. Beban Pertama

No	Urutan Proses Uji Coba	Percobaan				
		1	2	3	4	5
1	Gagang telepon diangkat	√	√	√	√	√
2	Memasukkan password dengan benar	√	√	√	√	√
3	Sinyal berpindah ke tegangan 12 volt DC	√	√	√	√	√
4	Muncul Nada 1	√	√	√	√	√
5	Muncul Nada 3	√	√	√	√	√
6	Memasukkan kode perintah (1-7-#)	√	√	√	√	√
7	Muncul Nada indikator 1 kali	√	√	√	√	√
8	Muncul Nada 6	√	√	√	√	√
9	Muncul Nada 4	√	√	√	√	√
10	Sinyal berpindah ke jaringan telepon	√	√	√	√	√

b. Beban Kedua

No	Urutan Proses Uji Coba	Percobaan				
		1	2	3	4	5
1	Gagang telepon diangkat	√	√	√	√	√

2	Memasukkan password dengan benar	√	√	√	√	√
3	Sinyal berpindah ke tegangan 12 volt DC	√	√	√	√	√
4	Muncul Nada 1	√	√	√	√	√
5	Muncul Nada 3	√	√	√	√	√
6	Memasukkan kode perintah (2-7-#)	√	√	√	√	√
7	Muncul Nada indikator 2 kali	√	√	√	√	√
8	Muncul Nada 6	√	√	√	√	√
9	Muncul Nada 4	√	√	√	√	√
10	Sinyal berpindah ke jaringan telepon	√	√	√	√	√

c. Beban Ketiga

No	**Urutan Proses Uji Coba**	**Percobaan**				
		1	**2**	**3**	**4**	**5**
1	Gagang telepon diangkat	√	√	√	√	√
2	Memasukkan password dengan benar	√	√	√	√	√
3	Sinyal berpindah ke tegangan 12 volt DC	√	√	√	√	√
4	Muncul Nada 1	√	√	√	√	√
5	Muncul Nada 3	√	√	√	√	√
6	Memasukkan kode perintah (3-7-#)	√	√	√	√	√
7	Muncul Nada indikator 3 kali	√	√	√	√	√
8	Muncul Nada 6	√	√	√	√	√
9	Muncul Nada 4	√	√	√	√	√
10	Sinyal berpindah ke jaringan telepon	√	√	√	√	√

d. Beban Keempat

No	Urutan Proses Uji Coba	Percobaan				
		1	2	3	4	5
1	Gagang telepon diangkat	√	√	√	√	√
2	Memasukkan password dengan benar	√	√	√	√	√
3	Sinyal berpindah ke tegangan 12 volt DC	√	√	√	√	√
4	Muncul Nada 1	√	√	√	√	√
5	Muncul Nada 3	√	√	√	√	√
6	Memasukkan kode perintah (4-7-#)	√	√	√	√	√
7	Muncul Nada indikator 4 kali	√	√	√	√	√
8	Muncul Nada 6	√	√	√	√	√
9	Muncul Nada 4	√	√	√	√	√
10	Sinyal berpindah ke jaringan telepon	√	√	√	√	√

e. Beban Kelima

No	Urutan Proses Uji Coba	Percobaan				
		1	2	3	4	5
1	Gagang telepon diangkat	√	√	√	√	√
2	Memasukkan password dengan benar	√	√	√	√	√
3	Sinyal berpindah ke tegangan 12 volt DC	√	√	√	√	√
4	Muncul Nada 1	√	√	√	√	√
5	Muncul Nada 3	√	√	√	√	√
6	Memasukkan kode perintah (5-7-#)	√	√	√	√	√

7	Muncul Nada indikator 5 kali	√	√	√	√	√
8	Muncul Nada 6	√	√	√	√	√
9	Muncul Nada 4	√	√	√	√	√
10	Sinyal berpindah ke STO	√	√	√	√	√

Uji Coba 2 Bagian Kedua - Pengendali Menanyakan Status Beban (Dalam Kondisi Aktif) Dan Selesai Memberikan Perintah

a. Beban Pertama

No	**Urutan Proses Uji Coba**	**Percobaan**				
		1	**2**	**3**	**4**	**5**
1	Gagang telepon diangkat	√	√	√	√	√
2	Memasukkan password dengan benar	√	√	√	√	√
3	Sinyal berpindah ke tegangan 12 volt DC	√	√	√	√	√
4	Muncul Nada 1	√	√	√	√	√
5	Muncul Nada 3	√	√	√	√	√
6	Memasukkan kode perintah (1-9-#)	√	√	√	√	√
7	Muncul Nada indikator 1 kali	√	√	√	√	√
8	Muncul Nada 6	√	√	√	√	√
9	Muncul Nada 4	√	√	√	√	√
10	Sinyal berpindah ke jaringan telepon	√	√	√	√	√

b. Beban Kedua

No	Urutan Proses Uji Coba	Percobaan				
		1	2	3	4	5
1	Gagang telepon diangkat	√	√	√	√	√
2	Memasukkan password dengan benar	√	√	√	√	√
3	Sinyal berpindah ke tegangan 12 volt DC	√	√	√	√	√
4	Muncul Nada 1	√	√	√	√	√
5	Muncul Nada 3	√	√	√	√	√
6	Memasukkan kode perintah (2-9-#)	√	√	√	√	√
7	Muncul Nada indikator 2 kali	√	√	√	√	√
8	Muncul Nada 6	√	√	√	√	√
9	Muncul Nada 4	√	√	√	√	√
10	Sinyal berpindah ke jaringan telepon	√	√	√	√	√

c. Beban Ketiga

No	Urutan Proses Uji Coba	Percobaan				
		1	2	3	4	5
1	Gagang telepon diangkat	√	√	√	√	√
2	Memasukkan password dengan benar	√	√	√	√	√
3	Sinyal berpindah ke tegangan 12 volt DC	√	√	√	√	√
4	Muncul Nada 1	√	√	√	√	√
5	Muncul Nada 3	√	√	√	√	√
6	Memasukkan kode perintah (3-9-#)	√	√	√	√	√

7	Muncul Nada indikator 3 kali	√	√	√	√	√
8	Muncul Nada 6	√	√	√	√	√
9	Muncul Nada 4	√	√	√	√	√
10	Sinyal berpindah ke jaringan telepon	√	√	√	√	√

d. Beban Keempat

No	**Urutan Proses Uji Coba**	**Percobaan**				
		1	**2**	**3**	**4**	**5**
1	Gagang telepon diangkat	√	√	√	√	√
2	Memasukkan password dengan benar	√	√	√	√	√
3	Sinyal berpindah ke tegangan 12 volt DC	√	√	√	√	√
4	Muncul Nada 1	√	√	√	√	√
5	Muncul Nada 3	√	√	√	√	√
6	Memasukkan kode perintah (4-9-#)	√	√	√	√	√
7	Muncul Nada indikator 4 kali	√	√	√	√	√
8	Muncul Nada 6	√	√	√	√	√
9	Muncul Nada 4	√	√	√	√	√
10	Sinyal berpindah ke jaringan telepon	√	√	√	√	√

e. Beban Kelima

No	Urutan Proses Uji Coba	Percobaan				
		1	2	3	4	5
1	Gagang telepon diangkat	√	√	√	√	√
2	Memasukkan password dengan benar	√	√	√	√	√
3	Sinyal berpindah ke tegangan 12 volt DC	√	√	√	√	√
4	Muncul Nada 1	√	√	√	√	√
5	Muncul Nada 3	√	√	√	√	√
6	Memasukkan kode perintah (5-9-#)	√	√	√	√	√
7	Muncul Nada indikator 5 kali	√	√	√	√	√
8	Muncul Nada 6	√	√	√	√	√
9	Muncul Nada 4	√	√	√	√	√
10	Sinyal berpindah ke jaringan telepon	√	√	√	√	√

Uji Coba 2 Bagian Ketiga - Pengendali Menonaktifkan Beban Dan Selesai Memberikan Perintah

a. Beban Pertama

No	Urutan Proses Uji Coba	Percobaan				
		1	2	3	4	5
1	Gagang telepon diangkat	√	√	√	√	√
2	Memasukkan password dengan benar	√	√	√	√	√
3	Sinyal berpindah ke tegangan 12 volt DC	√	√	√	√	√

4	Muncul Nada 1	√	√	√	√	√
5	Muncul Nada 3	√	√	√	√	√
6	Memasukkan kode perintah (1-8-#)	√	√	√	√	√
7	Muncul Nada indikator 1 kali	√	√	√	√	√
8	Muncul Nada 7	√	√	√	√	√
9	Muncul Nada 4	√	√	√	√	√
10	Sinyal berpindah ke jaringan telepon	√	√	√	√	√

b. Beban Kedua

No	**Urutan Proses Uji Coba**	**Percobaan**				
		1	**2**	**3**	**4**	**5**
1	Gagang telepon diangkat	√	√	√	√	√
2	Memasukkan password dengan benar	√	√	√	√	√
3	Sinyal berpindah ke tegangan 12 volt DC	√	√	√	√	√
4	Muncul Nada 1	√	√	√	√	√
5	Muncul Nada 3	√	√	√	√	√
6	Memasukkan kode perintah (2-8-#)	√	√	√	√	√
7	Muncul Nada indikator 2 kali	√	√	√	√	√
8	Muncul Nada 7	√	√	√	√	√
9	Muncul Nada 4	√	√	√	√	√
10	Sinyal berpindah ke jaringan telepon	√	√	√	√	√

c. Beban Ketiga

No	Urutan Proses Uji Coba	Percobaan				
		1	2	3	4	5
1	Gagang telepon diangkat	√	√	√	√	√
2	Memasukkan password dengan benar	√	√	√	√	√
3	Sinyal berpindah ke tegangan 12 volt DC	√	√	√	√	√
4	Muncul Nada 1	√	√	√	√	√
5	Muncul Nada 3	√	√	√	√	√
6	Memasukkan kode perintah (3-8-#)	√	√	√	√	√
7	Muncul Nada indikator 3 kali	√	√	√	√	√
8	Muncul Nada 7	√	√	√	√	√
9	Muncul Nada 4	√	√	√	√	√
10	Sinyal berpindah ke jaringan telepon	√	√	√	√	√

d. Beban Keempat

No	Urutan Proses Uji Coba	Percobaan				
		1	2	3	4	5
1	Gagang telepon diangkat	√	√	√	√	√
2	Memasukkan password dengan benar	√	√	√	√	√
3	Sinyal berpindah ke tegangan 12 volt DC	√	√	√	√	√
4	Muncul Nada 1	√	√	√	√	√
5	Muncul Nada 3	√	√	√	√	√
6	Memasukkan kode perintah (4-8-#)	√	√	√	√	√

7	Muncul Nada indikator 4 kali	√	√	√	√	√
8	Muncul Nada 7	√	√	√	√	√
9	Muncul Nada 4	√	√	√	√	√
10	Sinyal berpindah ke jaringan telepon	√	√	√	√	√

e. Beban Kelima

No	**Urutan Proses Uji Coba**	**Percobaan**				
		1	**2**	**3**	**4**	**5**
1	Gagang telepon diangkat	√	√	√	√	√
2	Memasukkan password dengan benar	√	√	√	√	√
3	Sinyal berpindah ke tegangan 12 volt DC	√	√	√	√	√
4	Muncul Nada 1	√	√	√	√	√
5	Muncul Nada 3	√	√	√	√	√
6	Memasukkan kode perintah (5-8-#)	√	√	√	√	√
7	Muncul Nada indikator 5 kali	√	√	√	√	√
8	Muncul Nada 7	√	√	√	√	√
9	Muncul Nada 4	√	√	√	√	√
10	Sinyal berpindah ke jaringan telepon	√	√	√	√	√

Tabel Uji Coba Sistem Pengendalian Secara Lokal

Uji Coba 2 Bagian Keempat - Pengendali Menanyakan Status Beban (Dalam Kondisi Nonaktif) Dan Selesai Memberikan Perintah

a. Beban Pertama

No	Urutan Proses Uji Coba	Percobaan				
		1	2	3	4	5
1	Gagang telepon diangkat	√	√	√	√	√
2	Memasukkan password dengan benar	√	√	√	√	√
3	Sinyal berpindah ke tegangan 12 volt DC	√	√	√	√	√
4	Muncul Nada 1	√	√	√	√	√
5	Muncul Nada 3	√	√	√	√	√
6	Memasukkan kode perintah (1-9-#)	√	√	√	√	√
7	Muncul Nada indikator 1 kali	√	√	√	√	√
8	Muncul Nada 7	√	√	√	√	√
9	Muncul Nada 4	√	√	√	√	√
10	Sinyal berpindah ke jaringan telepon	√	√	√	√	√

b. Beban Kedua

No	Urutan Proses Uji Coba	Percobaan				
		1	2	3	4	5
1	Gagang telepon diangkat	√	√	√	√	√

2	Memasukkan password dengan benar	√	√	√	√	√
3	Sinyal berpindah ke tegangan 12 volt DC	√	√	√	√	√
4	Muncul Nada 1	√	√	√	√	√
5	Muncul Nada 3	√	√	√	√	√
6	Memasukkan kode perintah (2-9-#)	√	√	√	√	√
7	Muncul Nada indikator 2 kali	√	√	√	√	√
8	Muncul Nada 7	√	√	√	√	√
9	Muncul Nada 4	√	√	√	√	√
10	Sinyal berpindah ke jaringan telepon	√	√	√	√	√

c. Beban Ketiga

No	**Urutan Proses Uji Coba**	**Percobaan**				
		1	**2**	**3**	**4**	**5**
1	Gagang telepon diangkat	√	√	√	√	√
2	Memasukkan password dengan benar	√	√	√	√	√
3	Sinyal berpindah ke tegangan 12 volt DC	√	√	√	√	√
4	Muncul Nada 1	√	√	√	√	√
5	Muncul Nada 3	√	√	√	√	√
6	Memasukkan kode perintah (3-9-#)	√	√	√	√	√
7	Muncul Nada indikator 3 kali	√	√	√	√	√
8	Muncul Nada 7	√	√	√	√	√
9	Muncul Nada 4	√	√	√	√	√
10	Sinyal berpindah ke jaringan telepon	√	√	√	√	√

d. Beban Keempat

No	Urutan Proses Uji Coba	Percobaan				
		1	2	3	4	5
1	Gagang telepon diangkat	√	√	√	√	√
2	Memasukkan password dengan benar	√	√	√	√	√
3	Sinyal berpindah ke tegangan 12 volt DC	√	√	√	√	√
4	Muncul Nada 1	√	√	√	√	√
5	Muncul Nada 3	√	√	√	√	√
6	Memasukkan kode perintah (4-9-#)	√	√	√	√	√
7	Muncul Nada indikator 4 kali	√	√	√	√	√
8	Muncul Nada 7	√	√	√	√	√
9	Muncul Nada 4	√	√	√	√	√
10	Sinyal berpindah ke jaringan telepon	√	√	√	√	√

e. Beban Kelima

No	Urutan Proses Uji Coba	Percobaan				
		1	2	3	4	5
1	Gagang telepon diangkat	√	√	√	√	√
2	Memasukkan password dengan benar	√	√	√	√	√
3	Sinyal berpindah ke tegangan 12 volt DC	√	√	√	√	√
4	Muncul Nada 1	√	√	√	√	√
5	Muncul Nada 3	√	√	√	√	√
6	Memasukkan kode perintah (5-9-#)	√	√	√	√	√

7	Muncul Nada indikator 5 kali	√	√	√	√	√
8	Muncul Nada 7	√	√	√	√	√
9	Muncul Nada 4	√	√	√	√	√
10	Sinyal berpindah ke jaringan telepon	√	√	√	√	√

Uji Coba 3 - Pengendali Salah Dalam Memasukkan Kode Perintah Sebanyak 3 Kali

No	**Urutan Proses Uji Coba**	**Percobaan**				
		1	**2**	**3**	**4**	**5**
1	Gagang telepon diangkat	√	√	√	√	√
2	Memasukkan password dengan benar	√	√	√	√	√
3	Sinyal berpindah ke tegangan 12 volt DC	√	√	√	√	√
4	Muncul Nada 1	√	√	√	√	√
5	Muncul Nada 3	√	√	√	√	√
6	Memasukkan kode perintah (pertama)	1-9-7	2-0-7	8-3-#	9-4-#	5-0-7
7	Muncul Nada 3	√	√	√	√	√
8	Memasukkan kode perintah (kedua)	9-1-7	7-0-2	3-#-8	9-#-4	8-5-#
9	Muncul Nada 3	√	√	√	√	√
10	Memasukkan kode perintah (ketiga)	7-1-9	0-2-7	8-#-3	4-#-9	0-9-5
11	Muncul Nada 4	√	√	√	√	√
12	Sinyal berpindah ke jaringan telepon	√	√	√	√	√

Tabel Uji Coba Sistem Pengendalian Secara Lokal

Uji Coba 4 - Pengendali Tidak Memasukkan Kode Perintah Selama 30 Detik

No	Urutan Proses Uji Coba	Percobaan				
		1	2	3	4	5
1	Gagang telepon diangkat	√	√	√	√	√
2	Memasukkan password dengan benar	√	√	√	√	√
3	Sinyal berpindah ke tegangan 12 volt DC	√	√	√	√	√
4	Muncul Nada 1	√	√	√	√	√
5	Muncul Nada 3	√	√	√	√	√
6	Tidak menekan tombol apapun selama 30 detik	√	√	√	√	√
7	Muncul Nada 4	√	√	√	√	√
8	Sinyal berpindah ke jaringan telepon	√	√	√	√	√

Uji Coba 5 - Pengendali Menekan Tombol # Sebagai Tombol Pertama Dalam Memasukkan Kode Perintah

No	Urutan Proses Uji Coba	Percobaan				
		1	2	3	4	5
1	Gagang telepon diangkat	√	√	√	√	√
2	Memasukkan password dengan benar	√	√	√	√	√
3	Sinyal berpindah ke tegangan 12 volt DC	√	√	√	√	√

4	Muncul Nada 1	√	√	√	√	√
5	Muncul Nada 3	√	√	√	√	√
6	Menekan tombol # sebanyak 1 kali	√	√	√	√	√
7	Muncul Nada 4	√	√	√	√	√
8	Sinyal berpindah ke jaringan telepon	√	√	√	√	√

Uji Coba 6 - Pengendali Salah Dalam Memasukkan Password Sebanyak 3 Kali

No	Urutan Proses Uji Coba	Percobaan				
		1	2	3	4	5
1	Gagang telepon diangkat	√	√	√	√	√
2	Memasukkan password	√	√	√	√	√
3	Muncul Nada 2	√	√	√	√	√

Ujicoba 7 - Pengendali Melakukan Panggilan Keluar

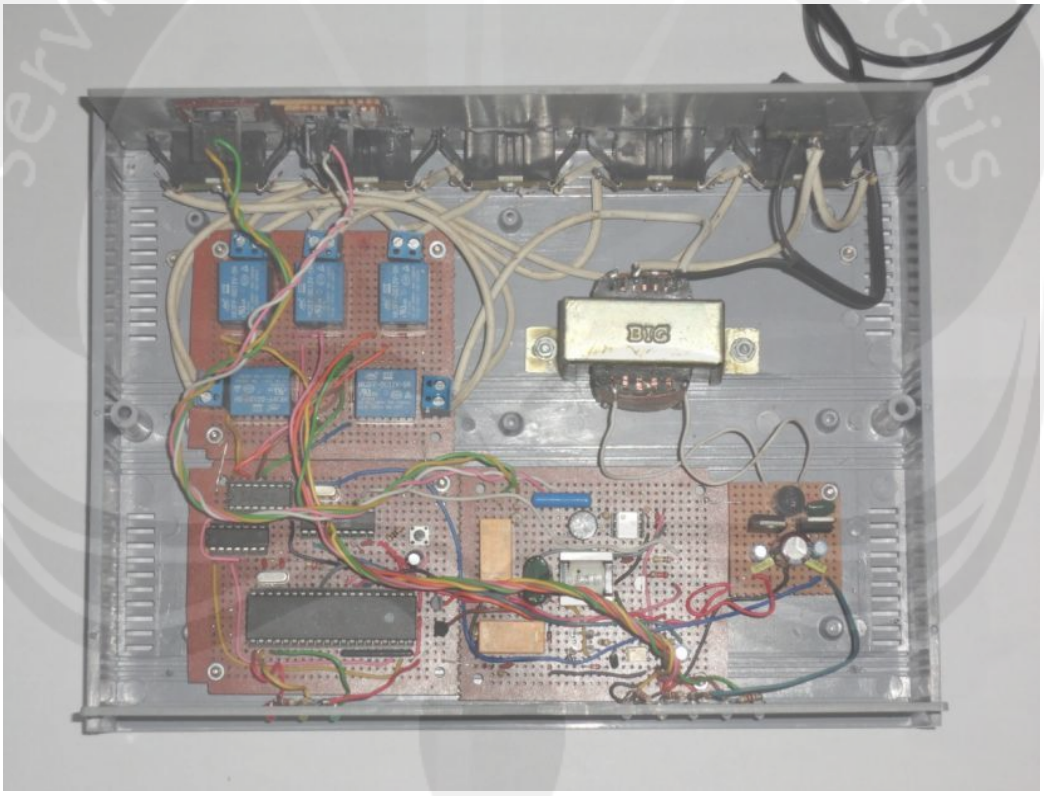
No	Urutan Proses Uji Coba	Percobaan				
		1	2	3	4	5
1	Gagang telepon diangkat	√	√	√	√	√
2	Memasukkan nomor telepon yang dituju	√	√	√	√	√
3	Sistem tidak bekerja	√	√	√	√	√
4	Sambungan telepon dimatikan / Gagang diletakkan	√	√	√	√	√
5	Sistem kembali bekerja	√	√	√	√	√

Lampiran 5. Foto Perangkat Keras Sistem Pengendali

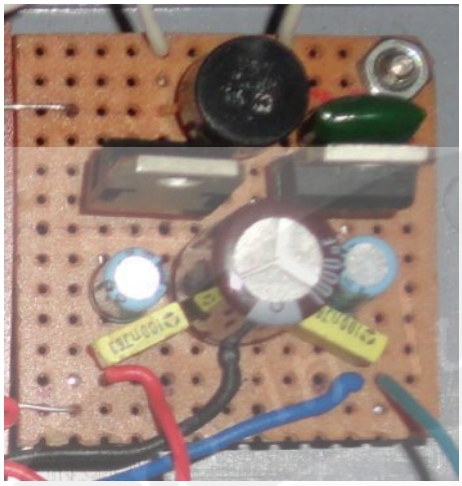
(a) Tampak Atas

(b) Tampak Depan

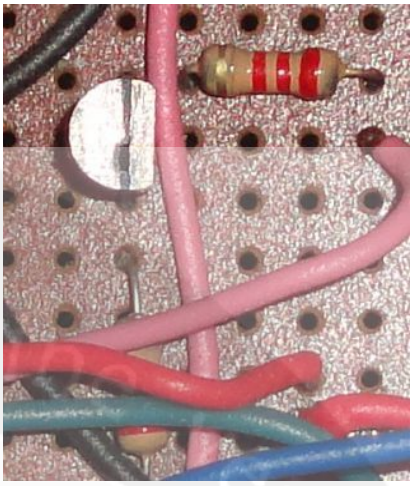
(c) Tampak Belakang



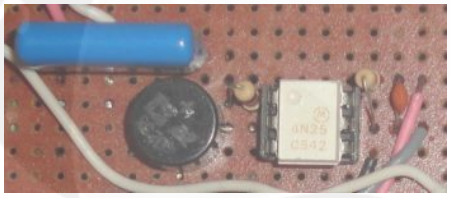
(d) Rangkaian Perangkat Keras



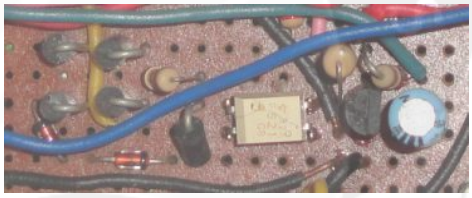
(e) Rangkaian Catu Daya



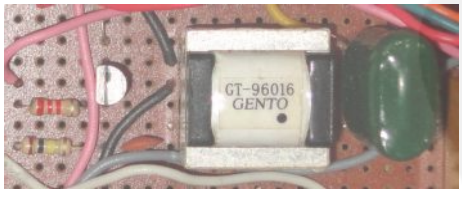
(f) Rangkaian Penggerak Nada Tanggapan



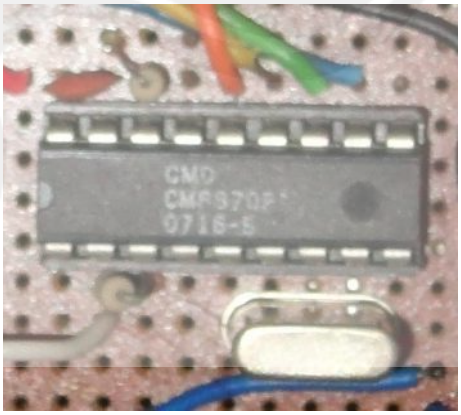
(g) Rangkaian Pendeteksi Dering



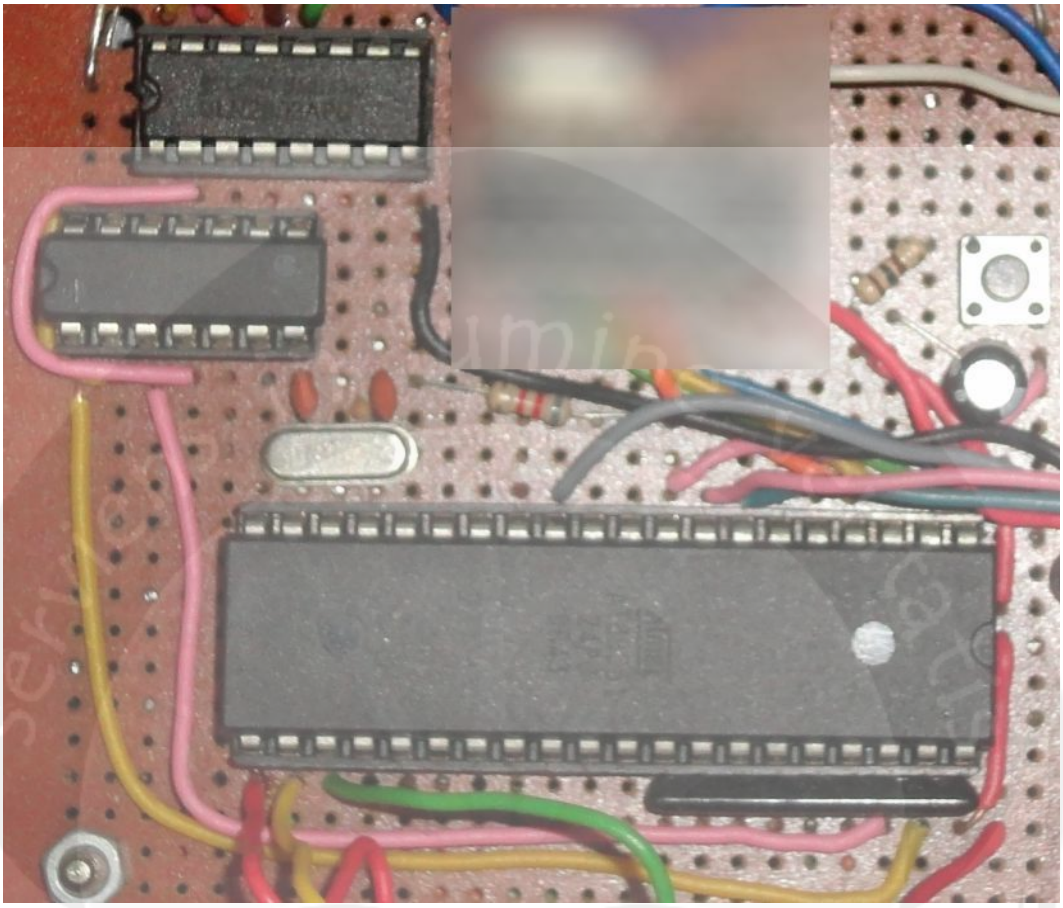
(h) Rangkaian Pendeteksi *Off-Hook*



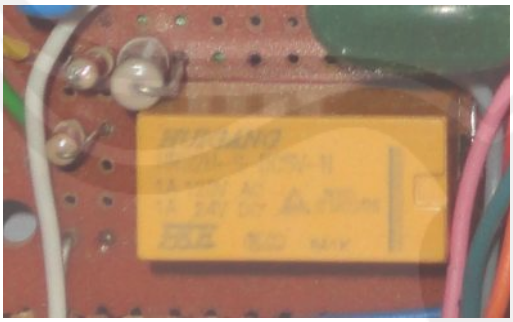
(i) Rangkaian Penerima Nada DTMF (1)



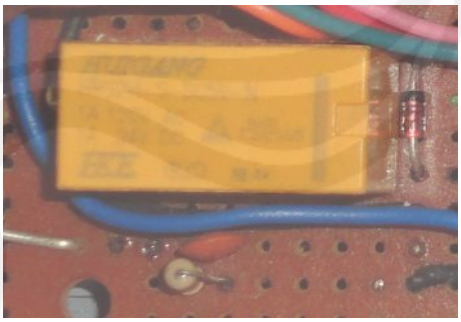
(j) Rangkaian Penerima Nada DTMF (2)



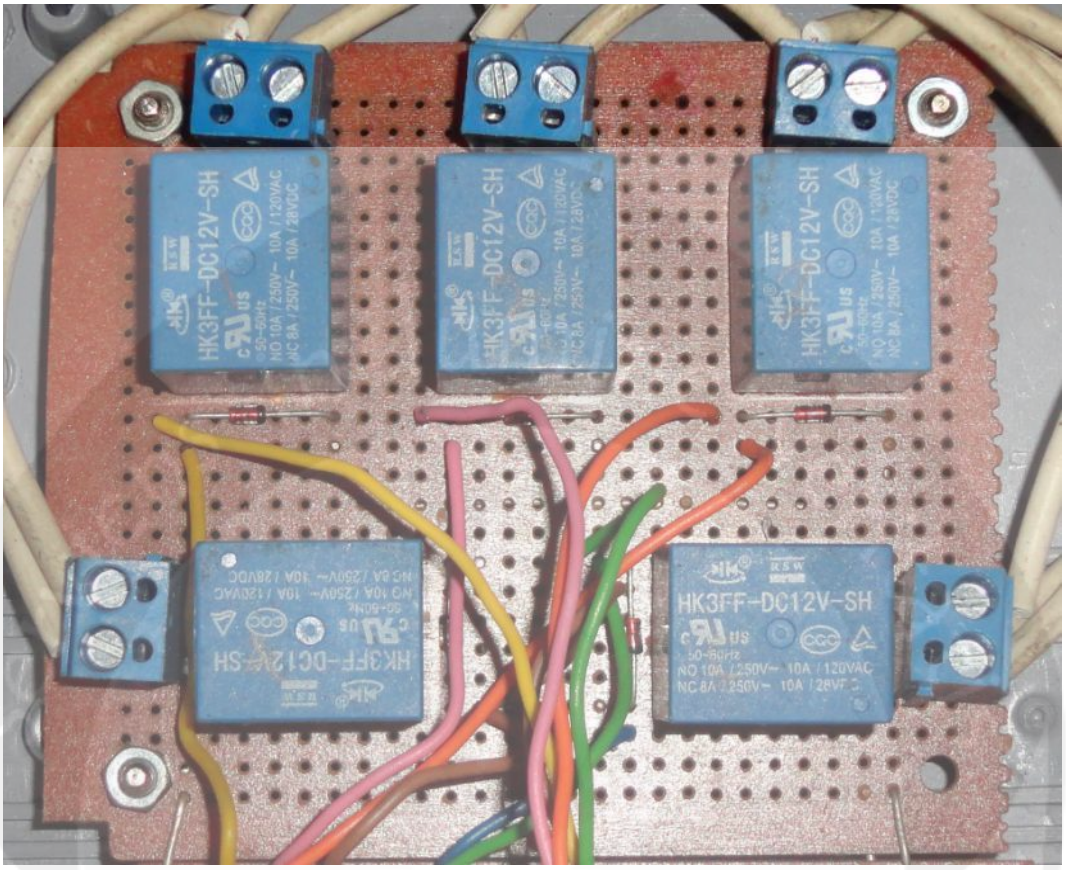
(k) Rangkaian Pengendali Utama



(l) Rangkaian Pengangkat Gagang Telepon



(m) Rangkaian Pemilih Sumber Sinyal Telepon



(n) Rangkaian Penggerak Relay Beban

Features

- Compatible with MCS®-51 Products
- 4K Bytes of In-System Programmable (ISP) Flash Memory
  - Endurance: 10,000 Write/Erase Cycles
- 4.0V to 5.5V Operating Range
- Fully Static Operation: 0 Hz to 33 MHz
- Three-level Program Memory Lock
- 128 x 8-bit Internal RAM
- 32 Programmable I/O Lines
- Two 16-bit Timer/Counters
- Six Interrupt Sources
- Full Duplex UART Serial Channel
- Low-power Idle and Power-down Modes
- Interrupt Recovery from Power-down Mode
- Watchdog Timer
- Dual Data Pointer
- Power-off Flag
- Fast Programming Time
- Flexible ISP Programming (Byte and Page Mode)
- Green (Pb/Halide-free) Packaging Option

8-bit Microcontroller with 4K Bytes In-System Programmable Flash

AT89S51

1. Description

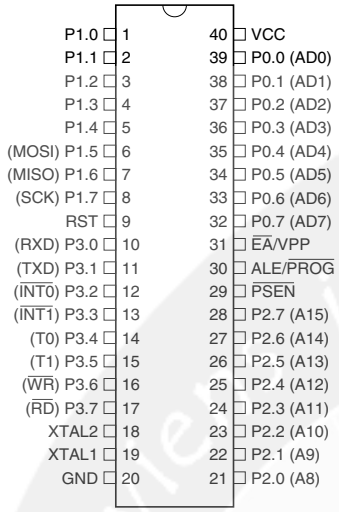
The AT89S51 is a low-power, high-performance CMOS 8-bit microcontroller with 4K bytes of In-System Programmable Flash memory. The device is manufactured using Atmel's high-density nonvolatile memory technology and is compatible with the industry-standard 80C51 instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with In-System Programmable Flash on a monolithic chip, the Atmel AT89S51 is a powerful microcontroller which provides a highly-flexible and cost-effective solution to many embedded control applications.

The AT89S51 provides the following standard features: 4K bytes of Flash, 128 bytes of RAM, 32 I/O lines, Watchdog timer, two data pointers, two 16-bit timer/counters, a five-vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator, and clock circuitry. In addition, the AT89S51 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and interrupt system to continue functioning. The Power-down mode saves the RAM contents but freezes the oscillator, disabling all other chip functions until the next external interrupt or hardware reset.

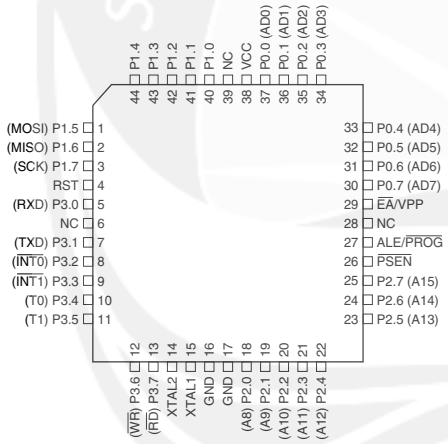
2487D–MICRO–6/08

2. Pin Configurations

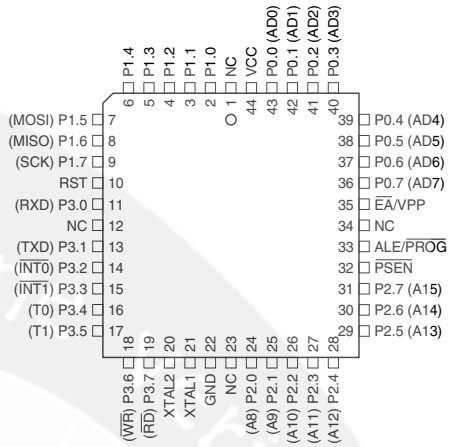
2.1 40-lead PDIP



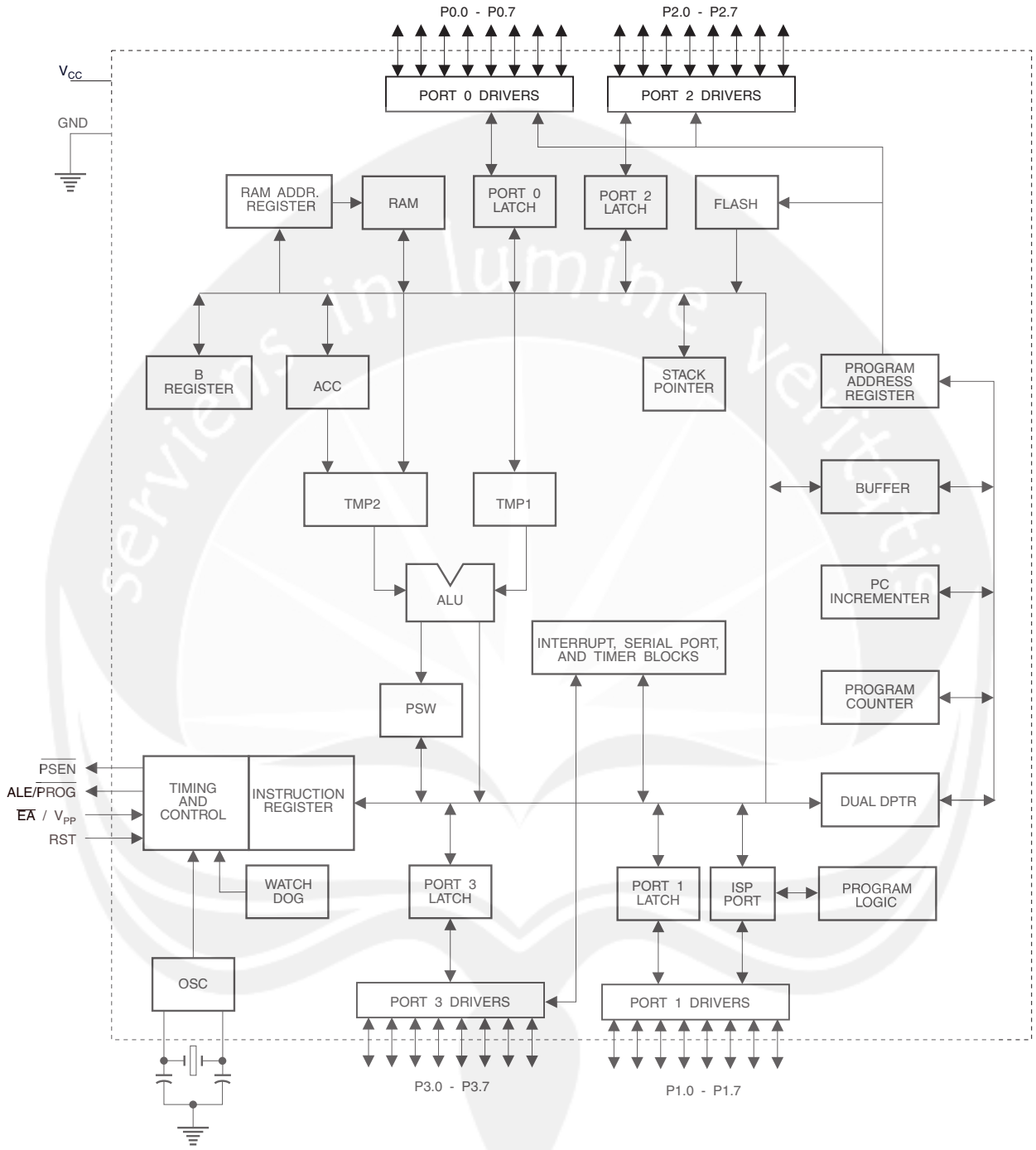
2.2 44-lead TQFP



2.3 44-lead PLCC



3. Block Diagram



4. Pin Description

4.1 VCC

Supply voltage.

4.2 GND

Ground.

4.3 Port 0

Port 0 is an 8-bit open drain bi-directional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pull-ups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. **External pull-ups are required during program verification**.

4.4 Port 1

Port 1 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 1 also receives the low-order address bytes during Flash programming and verification.

Port Pin	Alternate Functions
P1.5	MOSI (used for In-System Programming)
P1.6	MISO (used for In-System Programming)
P1.7	SCK (used for In-System Programming)

4.5 Port 2

Port 2 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

4.6 Port 3

Port 3 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the inter-

nal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pull-ups.

Port 3 receives some control signals for Flash programming and verification.

Port 3 also serves the functions of various special features of the AT89S51, as shown in the following table.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

4.7 RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. This pin drives High for 98 oscillator periods after the Watchdog times out. The DISRTO bit in SFR AUXR (address 8EH) can be used to disable this feature. In the default state of bit DISRTO, the RESET HIGH out feature is enabled.

4.8 ALE/$\overline{PROG}$

Address Latch Enable (ALE) is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

4.9 $\overline{PSEN}$

Program Store Enable ($\overline{PSEN}$) is the read strobe to external program memory.

When the AT89S51 is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory.

4.10 $\overline{EA}$/VPP

External Access Enable. $\overline{EA}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming.

4.11 XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

4.12 XTAL2

Output from the inverting oscillator amplifier

5. Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 5-1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

Table 5-1. AT89S51 SFR Map and Reset Values

0F8H									0FFH
0F0H	B 00000000								0F7H
0E8H									0EFH
0E0H	ACC 00000000								0E7H
0D8H									0DFH
0D0H	PSW 00000000								0D7H
0C8H									0CFH
0C0H									0C7H
0B8H	IP XX000000								0BFH
0B0H	P3 11111111								0B7H
0A8H	IE 0X000000								0AFH
0A0H	P2 11111111		AUXR1 XXXXXXX0				WDTRST XXXXXXXX		0A7H
98H	SCON 00000000	SBUF XXXXXXXX							9FH
90H	P1 11111111								97H
88H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000	AUXR XXX00XX0		8FH
80H	P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000		PCON 0XXX0000	87H

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Interrupt Registers: The individual interrupt enable bits are in the IE register. Two priorities can be set for each of the five interrupt sources in the IP register.

Table 5-2. AUXR: Auxiliary Register

AUXR Address = 8EH Reset Value = XXX00XX0B

Not Bit Addressable

	–	–	–	WDIDLE	DISRTO	–	–	DISALE
Bit	7	6	5	4	3	2	1	0

–	Reserved for future expansion
DISALE	Disable/Enable ALE
	DISALE Operating Mode
	0 ALE is emitted at a constant rate of 1/6 the oscillator frequency
	1 ALE is active only during a MOVX or MOVC instruction
DISRTO	Disable/Enable Reset-out
	DISRTO
	0 Reset pin is driven High after WDT times out
	1 Reset pin is input only
WDIDLE	Disable/Enable WDT in IDLE mode
WDIDLE	
0	WDT continues to count in IDLE mode
1	WDT halts counting in IDLE mode

Dual Data Pointer Registers: To facilitate accessing both internal and external data memory, two banks of 16-bit Data Pointer Registers are provided: DP0 at SFR address locations 82H-83H and DP1 at 84H-85H. Bit DPS = 0 in SFR AUXR1 selects DP0 and DPS = 1 selects DP1. The user should **ALWAYS** initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.

Power Off Flag: The Power Off Flag (POF) is located at bit 4 (PCON.4) in the PCON SFR. POF is set to “1” during power up. It can be set and rest under software control and is not affected by reset.

Table 5-3. AUXR1: Auxiliary Register 1

AUXR1 Address = A2H Reset Value = XXXXXXX0B

Not Bit Addressable

	–	–	–	–	–	–	–	DPS
Bit	7	6	5	4	3	2	1	0

– Reserved for future expansion

DPS Data Pointer Register Select

DPS	
0	Selects DPTR Registers DP0L, DP0H
1	Selects DPTR Registers DP1L, DP1H

6. Memory Organization

MCS-51 devices have a separate address space for Program and Data Memory. Up to 64K bytes each of external Program and Data Memory can be addressed.

6.1 Program Memory

If the $\overline{EA}$ pin is connected to GND, all program fetches are directed to external memory.

On the AT89S51, if $\overline{EA}$ is connected to V_{CC}, program fetches to addresses 0000H through FFFH are directed to internal memory and fetches to addresses 1000H through FFFFH are directed to external memory.

6.2 Data Memory

The AT89S51 implements 128 bytes of on-chip RAM. The 128 bytes are accessible via direct and indirect addressing modes. Stack operations are examples of indirect addressing, so the 128 bytes of data RAM are available as stack space.

7. Watchdog Timer (One-time Enabled with Reset-out)

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upsets. The WDT consists of a 14-bit counter and the Watchdog Timer Reset (WDTRST) SFR. The WDT is defaulted to disable from exiting reset. To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, it will increment every machine cycle while the oscillator is running. The WDT timeout period is dependent on the external clock frequency. There is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output RESET HIGH pulse at the RST pin.

7.1 Using the WDT

To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, the user needs to service it by writing 01EH and 0E1H to WDTRST to avoid a WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH), and this will reset the device. When the WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least

every 16383 machine cycles. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write-only register. The WDT counter cannot be read or written. When WDT overflows, it will generate an output RESET pulse at the RST pin. The RESET pulse duration is 98xTOSC, where TOSC = 1/FOSC. To make the best use of the WDT, it should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

7.2 WDT During Power-down and Idle

In Power-down mode the oscillator stops, which means the WDT also stops. While in Power-down mode, the user does not need to service the WDT. There are two methods of exiting Power-down mode: by a hardware reset or via a level-activated external interrupt, which is enabled prior to entering Power-down mode. When Power-down is exited with hardware reset, servicing the WDT should occur as it normally does whenever the AT89S51 is reset. Exiting Power-down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service for the interrupt used to exit Power-down mode.

To ensure that the WDT does not overflow within a few states of exiting Power-down, it is best to reset the WDT just before entering Power-down mode.

Before going into the IDLE mode, the WDIDLE bit in SFR AUXR is used to determine whether the WDT continues to count if enabled. The WDT keeps counting during IDLE (WDIDLE bit = 0) as the default state. To prevent the WDT from resetting the AT89S51 while in IDLE mode, the user should always set up a timer that will periodically exit IDLE, service the WDT, and reenter IDLE mode.

With WDIDLE bit enabled, the WDT will stop to count in IDLE mode and resumes the count upon exit from IDLE.

8. UART

The UART in the AT89S51 operates the same way as the UART in the AT89C51. For further information on the UART operation, please click on the document link below:

http://www.atmel.com/dyn/resources/prod_documents/DOC4316.PDF

9. Timer 0 and 1

Timer 0 and Timer 1 in the AT89S51 operate the same way as Timer 0 and Timer 1 in the AT89C51. For further information on the timers' operation, please click on the document link below:

http://www.atmel.com/dyn/resources/prod_documents/DOC4316.PDF

10. Interrupts

The AT89S51 has a total of five interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), two timer interrupts (Timers 0 and 1), and the serial port interrupt. These interrupts are all shown in Figure 10-1.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.

Note that Table 10-1 shows that bit positions IE.6 and IE.5 are unimplemented. User software should not write 1s to these bit positions, since they may be used in future AT89 products.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle.

Table 10-1. Interrupt Enable (IE) Register

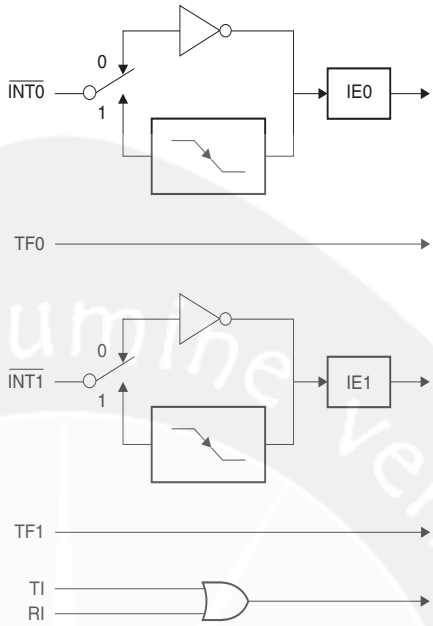
(MSB)							(LSB)
EA	–	–	ES	ET1	EX1	ET0	EX0

Enable Bit = 1 enables the interrupt.

Enable Bit = 0 disables the interrupt.

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
–	IE.6	Reserved
–	IE.5	Reserved
ES	IE.4	Serial Port interrupt enable bit
ET1	IE.3	Timer 1 interrupt enable bit
EX1	IE.2	External interrupt 1 enable bit
ET0	IE.1	Timer 0 interrupt enable bit
EX0	IE.0	External interrupt 0 enable bit
User software should never write 1s to reserved bits, because they may be used in future AT89 products.		

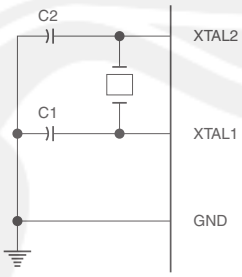
Figure 10-1. Interrupt Sources



11. Oscillator Characteristics

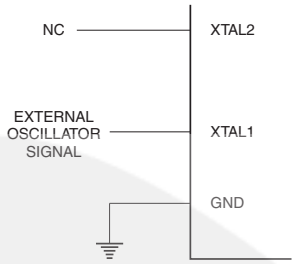
XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 11-1. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 11-2. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Figure 11-1. Oscillator Connections



Note: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

Figure 11-2. External Clock Drive Configuration



12. Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special function registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

13. Power-down Mode

In the Power-down mode, the oscillator is stopped, and the instruction that invokes Power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power-down mode is terminated. Exit from Power-down mode can be initiated either by a hardware reset or by activation of an enabled external interrupt ($\overline{INT0}$ or $\overline{INT1}$). Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Table 13-1. Status of External Pins During Idle and Power-down Modes

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

14. Program Memory Lock Bits

The AT89S51 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in Table 14-1.

Table 14-1. Lock Bit Protection Modes

Program Lock Bits				
	LB1	LB2	LB3	Protection Type
1	U	U	U	No program lock features
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash memory is disabled
3	P	P	U	Same as mode 2, but verify is also disabled
4	P	P	P	Same as mode 3, but external execution is also disabled

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of $\overline{EA}$ must agree with the current logic level at that pin in order for the device to function properly.

15. Programming the Flash – Parallel Mode

The AT89S51 is shipped with the on-chip Flash memory array ready to be programmed. The programming interface needs a high-voltage (12-volt) program enable signal and is compatible with conventional third-party Flash or EPROM programmers.

The AT89S51 code memory array is programmed byte-by-byte.

Programming Algorithm: Before programming the AT89S51, the address, data, and control signals should be set up according to the Flash Programming Modes table (Table 17-1) and Figure 17-1 and Figure 17-2. To program the AT89S51, take the following steps:

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ to 12V.
5. Pulse ALE/$\overline{PROG}$ once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 50 µs. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

$\overline{Data}$ Polling: The AT89S51 features $\overline{Data}$ Polling to indicate the end of a byte write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written data on P0.7. Once the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin. $\overline{Data}$ Polling may begin any time after a write cycle has been initiated.

Ready/$\overline{Busy}$: The progress of byte programming can also be monitored by the RDY/$\overline{BSY}$ output signal. P3.0 is pulled low after ALE goes high during programming to indicate $\overline{BUSY}$. P3.0 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. **The status of the individual lock bits can be verified directly by reading them back.**

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 000H, 100H, and 200H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

(000H) = 1EH indicates manufactured by Atmel
(100H) = 51H indicates AT89S51
(200H) = 06H

Chip Erase: In the parallel programming mode, a chip erase operation is initiated by using the proper combination of control signals and by pulsing ALE/$\overline{\text{PROG}}$ low for a duration of 200 ns - 500 ns.

In the serial programming mode, a chip erase operation is initiated by issuing the Chip Erase instruction. In this mode, chip erase is self-timed and takes about 500 ms.

During chip erase, a serial read from any address location will return 00H at the data output.

16. Programming the Flash – Serial Mode

The Code memory array can be programmed using the serial ISP interface while RST is pulled to V_{CC}. The serial interface consists of pins SCK, MOSI (input) and MISO (output). After RST is set high, the Programming Enable instruction needs to be executed first before other operations can be executed. Before a reprogramming sequence can occur, a Chip Erase operation is required.

The Chip Erase operation turns the content of every memory location in the Code array into FFH.

Either an external system clock can be supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The maximum serial clock (SCK) frequency should be less than 1/16 of the crystal frequency. With a 33 MHz oscillator clock, the maximum SCK frequency is 2 MHz.

16.1 Serial Programming Algorithm

To program and verify the AT89S51 in the serial programming mode, the following sequence is recommended:

1. Power-up sequence:
   a. Apply power between VCC and GND pins.
   b. Set RST pin to “H”.

If a crystal is not connected across pins XTAL1 and XTAL2, apply a 3 MHz to 33 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.

2. Enable serial programming by sending the Programming Enable serial instruction to pin MOSI/P1.5. The frequency of the shift clock supplied at pin SCK/P1.7 needs to be less than the CPU clock at XTAL1 divided by 16.
3. The Code array is programmed one byte at a time in either the Byte or Page mode. The write cycle is self-timed and typically takes less than 0.5 ms at 5V.
4. Any memory location can be verified by using the Read instruction that returns the content at the selected address at serial output MISO/P1.6.

5. At the end of a programming session, RST can be set low to commence normal device operation.

Power-off sequence (if needed):

1. Set XTAL1 to “L” (if a crystal is not used).
2. Set RST to “L”.
3. Turn V_{CC} power off.

Data Polling: The $\overline{\text{Data}}$ Polling feature is also available in the serial mode. In this mode, during a write cycle an attempted read of the last byte written will result in the complement of the MSB of the serial output byte on MISO.

16.2 Serial Programming Instruction Set

The Instruction Set for Serial Programming follows a 4-byte protocol and is shown in the ”Serial Programming Instruction Set” on page 20.

17. Programming Interface – Parallel Mode

Every code byte in the Flash array can be programmed by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

Most major worldwide programming vendors offer worldwide support for the Atmel AT89 microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Table 17-1. Flash Programming Modes

Mode	V_{CC}	RST	$\overline{\text{PSEN}}$	ALE/$\overline{\text{PROG}}$	$\overline{\text{EA}}$/V_{PP}	P2.6	P2.7	P3.3	P3.6	P3.7	P0.7-0 Data	P2.3-0 Address	P1.7-0 Address
Write Code Data	5V	H	L	(2)	12V	L	H	H	H	H	D_{IN}	A11-8	A7-0
Read Code Data	5V	H	L	H	H	L	L	L	H	H	D_{OUT}	A11-8	A7-0
Write Lock Bit 1	5V	H	L	(3)	12V	H	H	H	H	H	X	X	X
Write Lock Bit 2	5V	H	L	(3)	12V	H	H	H	L	L	X	X	X
Write Lock Bit 3	5V	H	L	(3)	12V	H	L	H	H	L	X	X	X
Read Lock Bits 1, 2, 3	5V	H	L	H	H	H	H	L	H	L	P0.2, P0.3, P0.4	X	X
Chip Erase	5V	H	L	(1)	12V	H	L	H	L	L	X	X	X
Read Atmel ID	5V	H	L	H	H	L	L	L	L	L	1EH	0000	00H
Read Device ID	5V	H	L	H	H	L	L	L	L	L	51H	0001	00H
Read Device ID	5V	H	L	H	H	L	L	L	L	L	06H	0010	00H

Notes:
1. Each $\overline{\text{PROG}}$ pulse is 200 ns - 500 ns for Chip Erase.
2. Each $\overline{\text{PROG}}$ pulse is 200 ns - 500 ns for Write Code Data.
3. Each $\overline{\text{PROG}}$ pulse is 200 ns - 500 ns for Write Lock Bits.
4. RDY/$\overline{\text{BSY}}$ signal is output on P3.0 during programming.
5. X = don’t care.

Figure 17-1. Programming the Flash Memory (Parallel Mode)

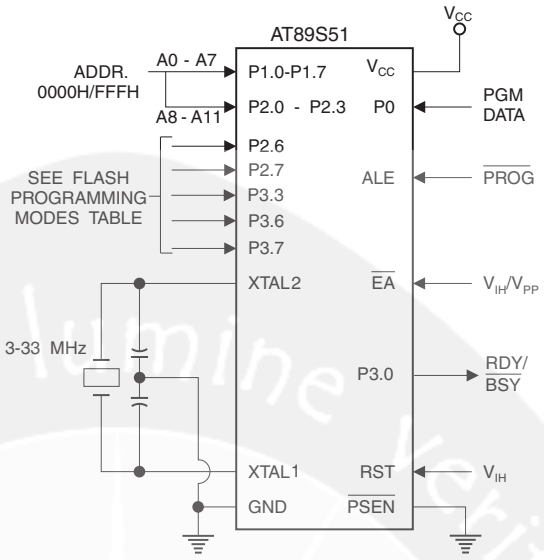
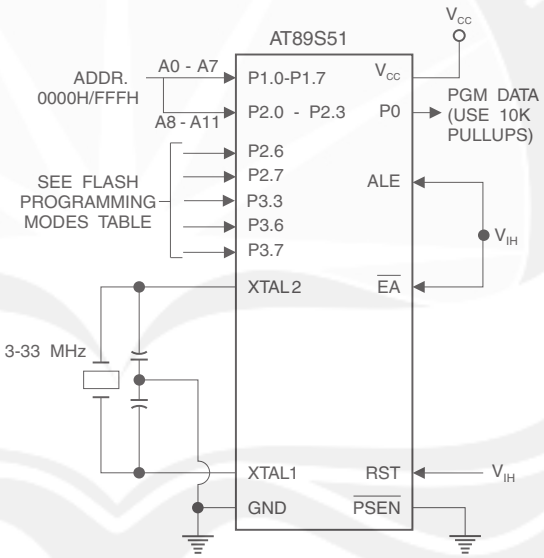


Figure 17-2. Verifying the Flash Memory (Parallel Mode)



18. Flash Programming and Verification Characteristics (Parallel Mode)

T_A = 20°C to 30°C, V_{CC} = 4.5 to 5.5V

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	11.5	12.5	V
I_{PP}	Programming Supply Current		10	mA
I_{CC}	V_{CC} Supply Current		30	mA
$1/t_{CLCL}$	Oscillator Frequency	3	33	MHz
t_{AVGL}	Address Setup to $\overline{PROG}$ Low	48 t_{CLCL}		
t_{GHAX}	Address Hold After $\overline{PROG}$	48 t_{CLCL}		
t_{DVGL}	Data Setup to $\overline{PROG}$ Low	48 t_{CLCL}		
t_{GHDX}	Data Hold After $\overline{PROG}$	48 t_{CLCL}		
t_{EHSH}	P2.7 ($\overline{ENABLE}$) High to V_{PP}	48 t_{CLCL}		
t_{SHGL}	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
t_{GHSL}	V_{PP} Hold After $\overline{PROG}$	10		µs
t_{GLGH}	$\overline{PROG}$ Width	0.2	1	µs
t_{AVQV}	Address to Data Valid		48t_{CLCL}	
t_{ELQV}	$\overline{ENABLE}$ Low to Data Valid		48t_{CLCL}	
t_{EHQZ}	Data Float After $\overline{ENABLE}$	0	48t_{CLCL}	
t_{GHBL}	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
t_{WC}	Byte Write Cycle Time		50	µs

Figure 18-1. Flash Programming and Verification Waveforms – Parallel Mode

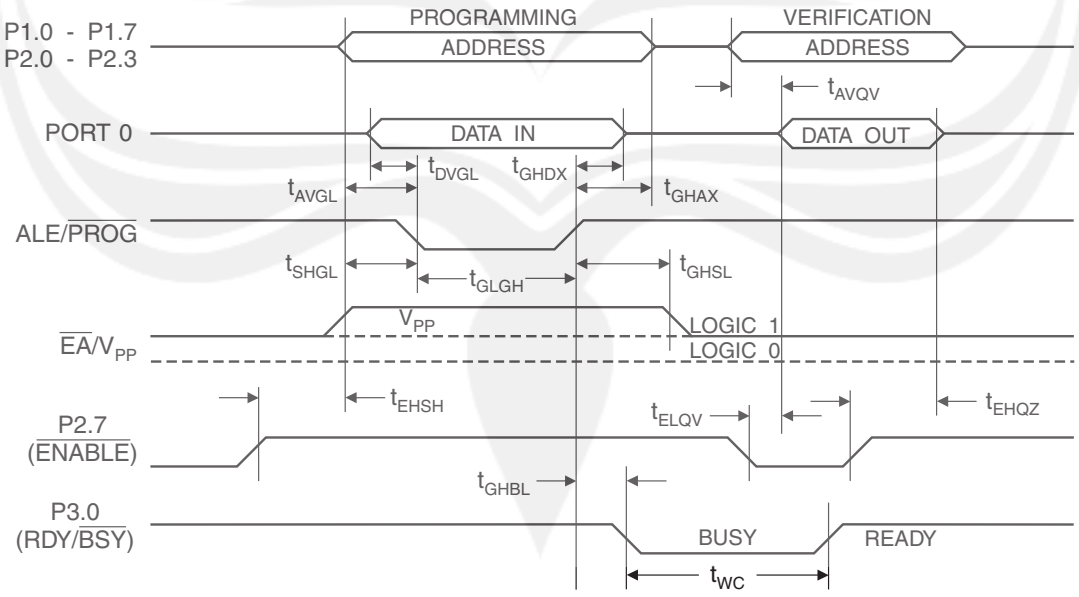
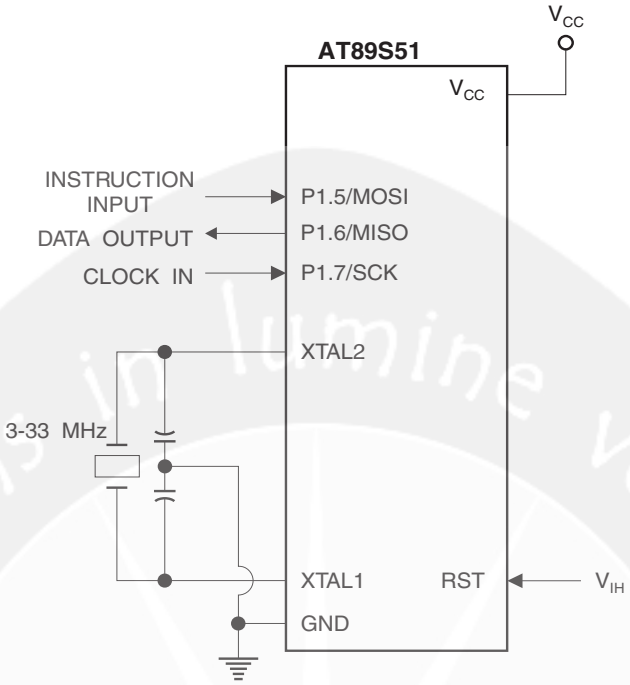
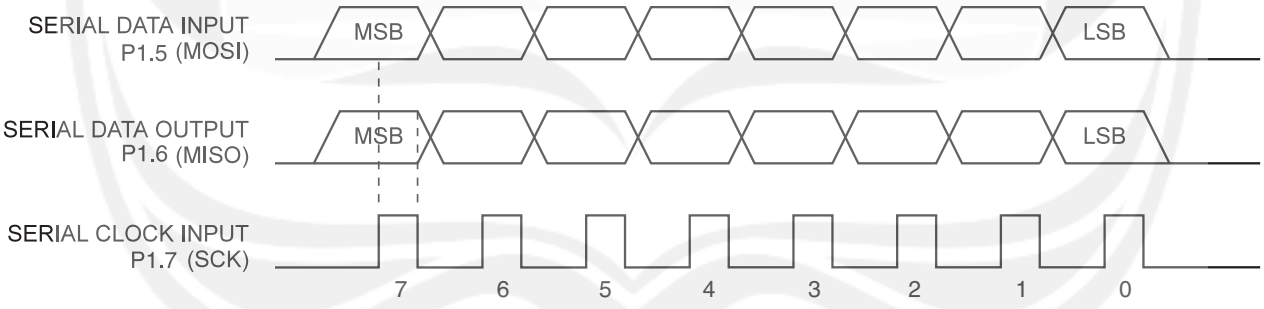


Figure 18-2. Flash Memory Serial Downloading



19. Flash Programming and Verification Waveforms – Serial Mode

Figure 19-1. Serial Programming Waveforms



20. Serial Programming Instruction Set

Instruction	Instruction Format				Operation
	Byte 1	Byte 2	Byte 3	Byte 4	
Programming Enable	1010 1100	0101 0011	xxxx xxxx	xxxx xxxx 0110 1001 (Output on MISO)	Enable Serial Programming while RST is high
Chip Erase	1010 1100	100x xxxx	xxxx xxxx	xxxx xxxx	Chip Erase Flash memory array
Read Program Memory (Byte Mode)	0010 0000	xxxx A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	Read data from Program memory in the byte mode
Write Program Memory (Byte Mode)	0100 0000	xxxx A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	Write data to Program memory in the byte mode
Write Lock Bits[1]	1010 1100	1110 00 B1 B2	xxxx xxxx	xxxx xxxx	Write Lock bits. See Note (1).
Read Lock Bits	0010 0100	xxxx xxxx	xxxx xxxx	xxx LB3 LB2 LB1 xx	Read back current status of the lock bits (a programmed lock bit reads back as a “1”)
Read Signature Bytes	0010 1000	xxxx A11 A10 A9 A8	A7 xxx xxx0	Signature Byte	Read Signature Byte
Read Program Memory (Page Mode)	0011 0000	xxxx A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Read data from Program memory in the Page Mode (256 bytes)
Write Program Memory (Page Mode)	0101 0000	xxxx A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Write data to Program memory in the Page Mode (256 bytes)

Note: 1. B1 = 0, B2 = 0 → Mode 1, no lock protection
B1 = 0, B2 = 1 → Mode 2, lock bit 1 activated
B1 = 1, B2 = 0 → Mode 3, lock bit 2 activated
B1 = 1, B2 = 1 → Mode 4, lock bit 3 activated

} Each of the lock bit modes need to be activated sequentially before Mode 4 can be executed.

After Reset signal is high, SCK should be low for at least 64 system clocks before it goes high to clock in the enable data bytes. No pulsing of Reset signal is necessary. SCK should be no faster than 1/16 of the system clock at XTAL1.

For Page Read/Write, the data always starts from byte 0 to 255. After the command byte and upper address byte are latched, each byte thereafter is treated as data until all 256 bytes are shifted in/out. Then the next instruction will be ready to be decoded.

21. Serial Programming Characteristics

Figure 21-1. Serial Programming Timing

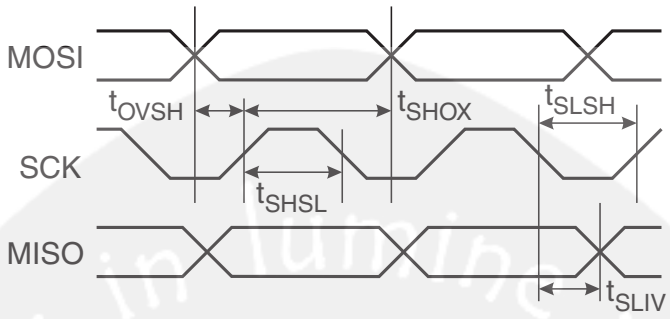


Table 21-1. Serial Programming Characteristics, T_A = -40· C to 85· C, V_{CC} = 4.0 - 5.5V (Unless Otherwise Noted)

Symbol	Parameter	Min	Typ	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	3		33	MHz
t_{CLCL}	Oscillator Period	30			ns
t_{SHSL}	SCK Pulse Width High	8 t_{CLCL}			ns
t_{SLSH}	SCK Pulse Width Low	8 t_{CLCL}			ns
t_{OVSH}	MOSI Setup to SCK High	t_{CLCL}			ns
t_{SHOX}	MOSI Hold after SCK High	2 t_{CLCL}			ns
t_{SLIV}	SCK Low to MISO Valid	10	16	32	ns
t_{ERASE}	Chip Erase Instruction Cycle Time			500	ms
t_{SWC}	Serial Byte Write Cycle Time			64 t_{CLCL} + 400	µs

22. Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.6V
DC Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

23. DC Characteristics

The values shown in this table are valid for T_A = -40°C to 85°C and V_{CC} = 4.0V to 5.5V, unless otherwise noted.

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low Voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC}-0.1	V
V_{IL1}	Input Low Voltage ($\overline{EA}$)		-0.5	0.2 V_{CC}-0.3	V
V_{IH}	Input High Voltage	(Except XTAL1, RST)	0.2 V_{CC}+0.9	V_{CC}+0.5	V
V_{IH1}	Input High Voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC}+0.5	V
V_{OL}	Output Low Voltage[1] (Ports 1,2,3)	I_{OL} = 1.6 mA		0.45	V
V_{OL1}	Output Low Voltage[1] (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.45	V
V_{OH}	Output High Voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ±10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ±10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
I_{IL}	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, V_{CC} = 5V ±10%		-300	µA
I_{LI}	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
RRST	Reset Pulldown Resistor		50	300	KΩ
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{CC}	Power Supply Current	Active Mode, 12 MHz		25	mA
		Idle Mode, 12 MHz		6.5	mA
	Power-down Mode[2]	V_{CC} = 5.5V		50	µA

Notes:
1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum I_{OL} per 8-bit port:
   Port 0: 26 mA Ports 1, 2, 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power-down is 2V.

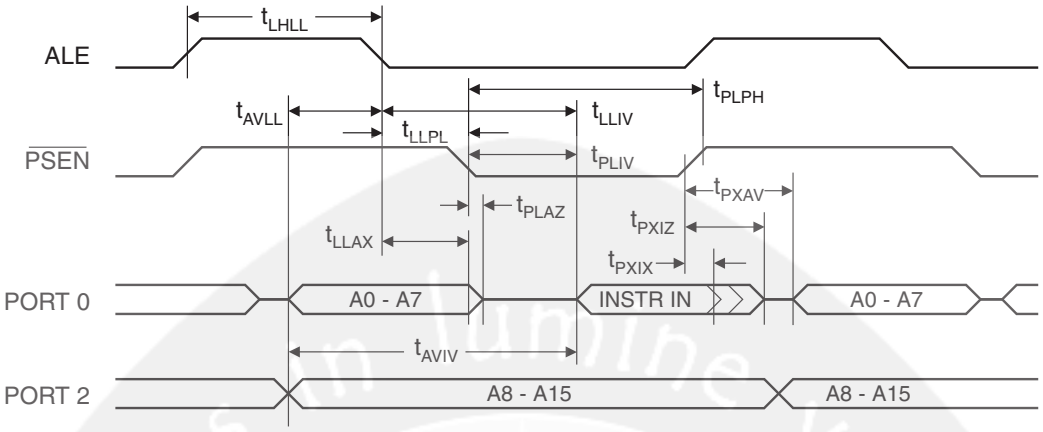
24. AC Characteristics

Under operating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; load capacitance for all other outputs = 80 pF.

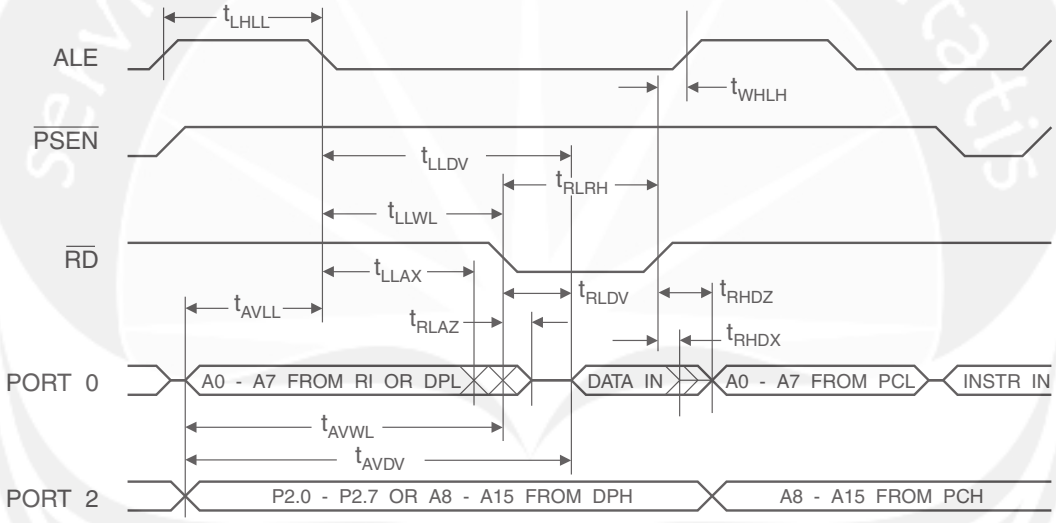
24.1 External Program and Data Memory Characteristics

Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
$1/t_{CLCL}$	Oscillator Frequency			0	33	MHz
t_{LHLL}	ALE Pulse Width	127		$2\ t_{CLCL}-40$		ns
t_{AVLL}	Address Valid to ALE Low	43		$t_{CLCL}-25$		ns
t_{LLAX}	Address Hold After ALE Low	48		$t_{CLCL}-25$		ns
t_{LLIV}	ALE Low to Valid Instruction In		233		$4\ t_{CLCL}-65$	ns
t_{LLPL}	ALE Low to $\overline{PSEN}$ Low	43		$t_{CLCL}-25$		ns
t_{PLPH}	$\overline{PSEN}$ Pulse Width	205		$3\ t_{CLCL}-45$		ns
t_{PLIV}	$\overline{PSEN}$ Low to Valid Instruction In		145		$3\ t_{CLCL}-60$	ns
t_{PXIX}	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
t_{PXIZ}	Input Instruction Float After $\overline{PSEN}$		59		$t_{CLCL}-25$	ns
t_{PXAV}	$\overline{PSEN}$ to Address Valid	75		$t_{CLCL}-8$		ns
t_{AVIV}	Address to Valid Instruction In		312		$5\ t_{CLCL}-80$	ns
t_{PLAZ}	$\overline{PSEN}$ Low to Address Float		10		10	ns
t_{RLRH}	$\overline{RD}$ Pulse Width	400		$6\ t_{CLCL}-100$		ns
t_{WLWH}	$\overline{WR}$ Pulse Width	400		$6\ t_{CLCL}-100$		ns
t_{RLDV}	$\overline{RD}$ Low to Valid Data In		252		$5\ t_{CLCL}-90$	ns
t_{RHDX}	Data Hold After $\overline{RD}$	0		0		ns
t_{RHDZ}	Data Float After $\overline{RD}$		97		$2\ t_{CLCL}-28$	ns
t_{LLDV}	ALE Low to Valid Data In		517		$8\ t_{CLCL}-150$	ns
t_{AVDV}	Address to Valid Data In		585		$9\ t_{CLCL}-165$	ns
t_{LLWL}	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	$3\ t_{CLCL}-50$	$3\ t_{CLCL}+50$	ns
t_{AVWL}	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		$4\ t_{CLCL}-75$		ns
t_{QVWX}	Data Valid to $\overline{WR}$ Transition	23		$t_{CLCL}-30$		ns
t_{QVWH}	Data Valid to $\overline{WR}$ High	433		$7\ t_{CLCL}-130$		ns
t_{WHQX}	Data Hold After $\overline{WR}$	33		$t_{CLCL}-25$		ns
t_{RLAZ}	$\overline{RD}$ Low to Address Float		0		0	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	$t_{CLCL}-25$	$t_{CLCL}+25$	ns

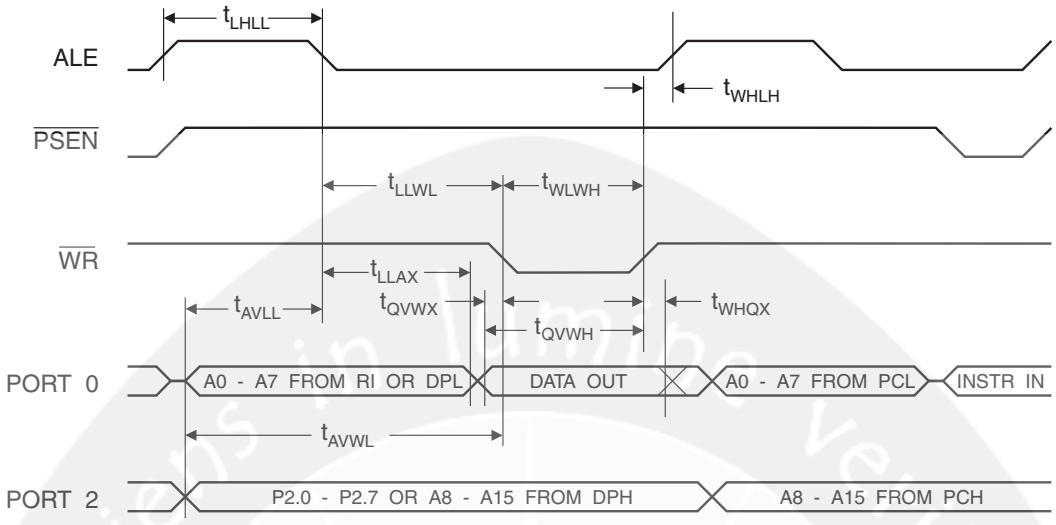
25. External Program Memory Read Cycle



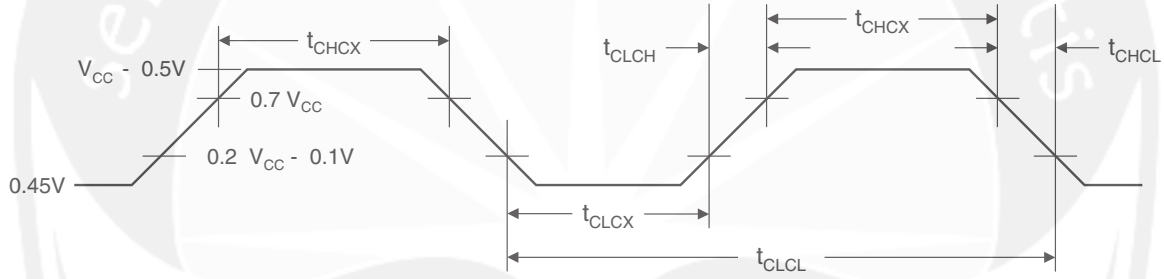
26. External Data Memory Read Cycle



27. External Data Memory Write Cycle



28. External Clock Drive Waveforms



29. External Clock Drive

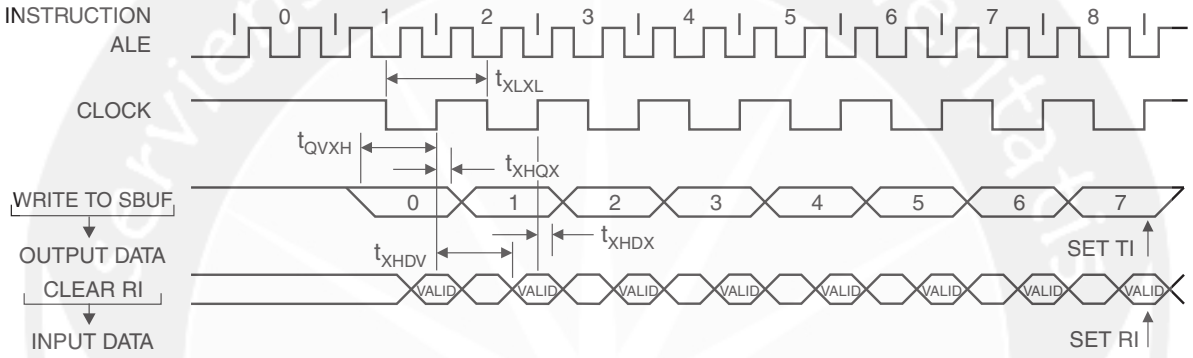
Symbol	Parameter	Min	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	0	33	MHz
t_{CLCL}	Clock Period	30		ns
t_{CHCX}	High Time	12		ns
t_{CLCX}	Low Time	12		ns
t_{CLCH}	Rise Time		5	ns
t_{CHCL}	Fall Time		5	ns

30. Serial Port Timing: Shift Register Mode Test Conditions

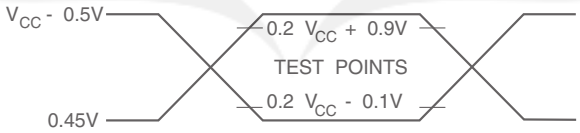
The values in this table are valid for V_{CC} = 4.0V to 5.5V and Load Capacitance = 80 pF.

Symbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
t_{XLXL}	Serial Port Clock Cycle Time	1.0		12 t_{CLCL}		µs
t_{QVXH}	Output Data Setup to Clock Rising Edge	700		10 t_{CLCL}-133		ns
t_{XHQX}	Output Data Hold After Clock Rising Edge	50		2 t_{CLCL}-80		ns
t_{XHDX}	Input Data Hold After Clock Rising Edge	0		0		ns
t_{XHDV}	Clock Rising Edge to Input Data Valid		700		10 t_{CLCL}-133	ns

31. Shift Register Mode Timing Waveforms

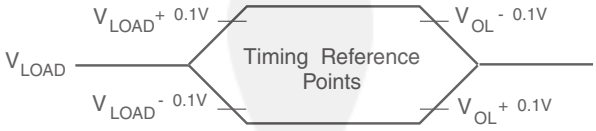


32. AC Testing Input/Output Waveforms[1]



Note: 1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

33. Float Waveforms[1]



Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

34. Ordering Information

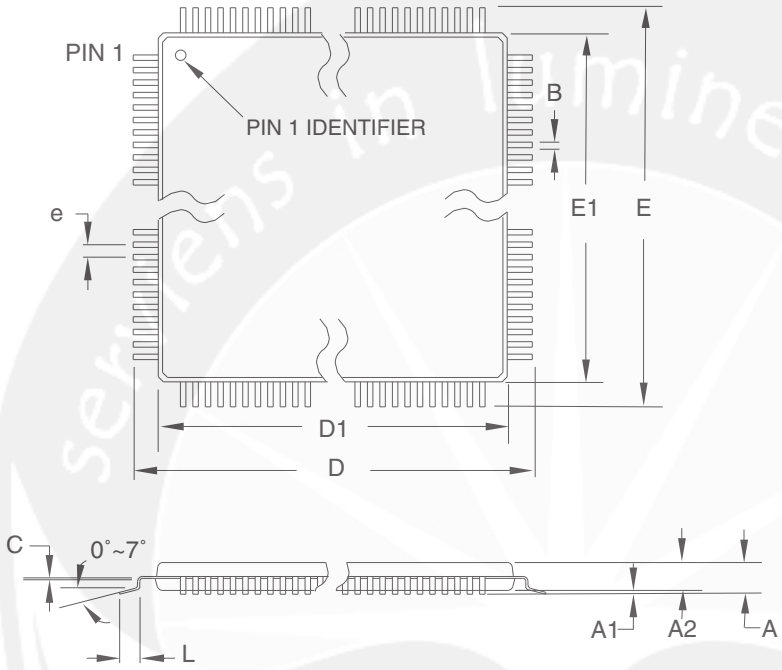
34.1 Green Package Option (Pb/Halide-free)

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
24	4.0V to 5.5V	AT89S51-24AU AT89S51-24JU AT89S51-24PU	44A 44J 40P6	Industrial (-40° C to 85° C)
33	4.5V to 5.5V	AT89S51-33AU AT89S51-33JU AT89S51-33PU	44A 44J 40P6	Industrial (-40° C to 85° C)

	Package Type
44A	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
44J	44-lead, Plastic J-leaded Chip Carrier (PLCC)
40P6	40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)

35. Packaging Information

35.1 44A – TQFP



COMMON DIMENSIONS
(Unit of Measure = mm)

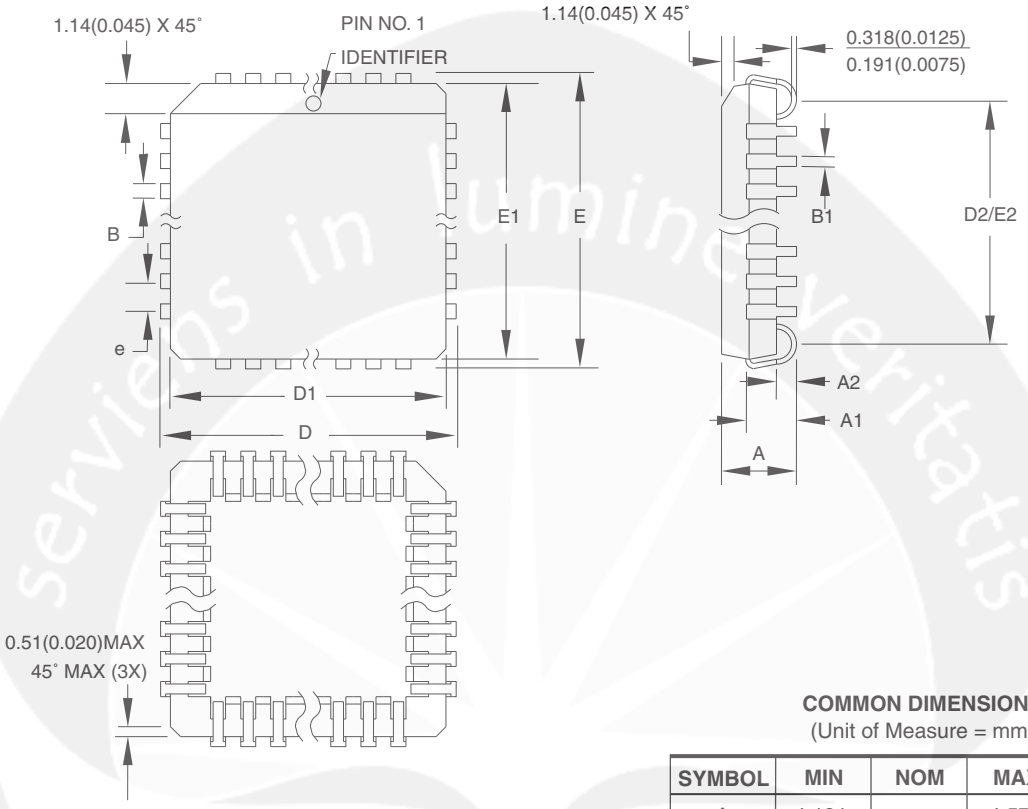
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	11.75	12.00	12.25	
D1	9.90	10.00	10.10	Note 2
E	11.75	12.00	12.25	
E1	9.90	10.00	10.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation ACB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10 mm maximum.

10/5/2001

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**44A,** 44-lead, 10 x 10 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	44A	B

35.2 44J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

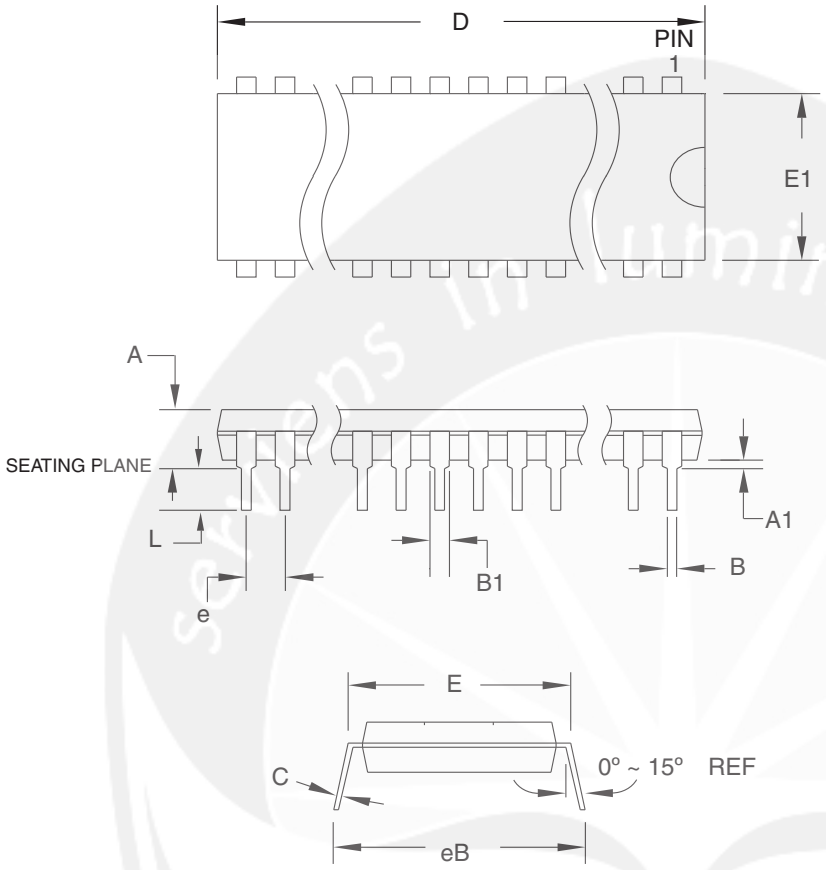
SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	17.399	–	17.653	
D1	16.510	–	16.662	Note 2
E	17.399	–	17.653	
E1	16.510	–	16.662	Note 2
D2/E2	14.986	–	16.002	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes:
1. This package conforms to JEDEC reference MS-018, Variation AC.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**44J**, 44-lead, Plastic J-leaded Chip Carrier (PLCC)	44J	B

35.3 40P6 – PDIP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	4.826	
A1	0.381	–	–	
D	52.070	–	52.578	Note 2
E	15.240	–	15.875	
E1	13.462	–	13.970	Note 2
B	0.356	–	0.559	
B1	1.041	–	1.651	
L	3.048	–	3.556	
C	0.203	–	0.381	
eB	15.494	–	17.526	
e	2.540 TYP			

Notes:
1. This package conforms to JEDEC reference MS-011, Variation AC.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

09/28/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**40P6**, 40-lead (0.600"/15.24 mm Wide) Plastic Dual Inline Package (PDIP)	40P6	B

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CMOS Integrated DTMF Receiver

Features

- Full DTMF receiver
- Less than 35mW power consumption
- Industrial temperature range
- Uses quartz crystal or ceramic resonators
- Adjustable acquisition and release times
- 18-pin DIP, 18-pin DIP EIAJ, 18-pin SOIC, 20-pin PLCC
- **CM8870C**
  - Power down mode
  - Inhibit mode
  - Buffered OSC3 output (PLCC package only)
- CM8870C is fully compatible with CM8870 for 18-pin devices by grounding pin 5 and pin 6.

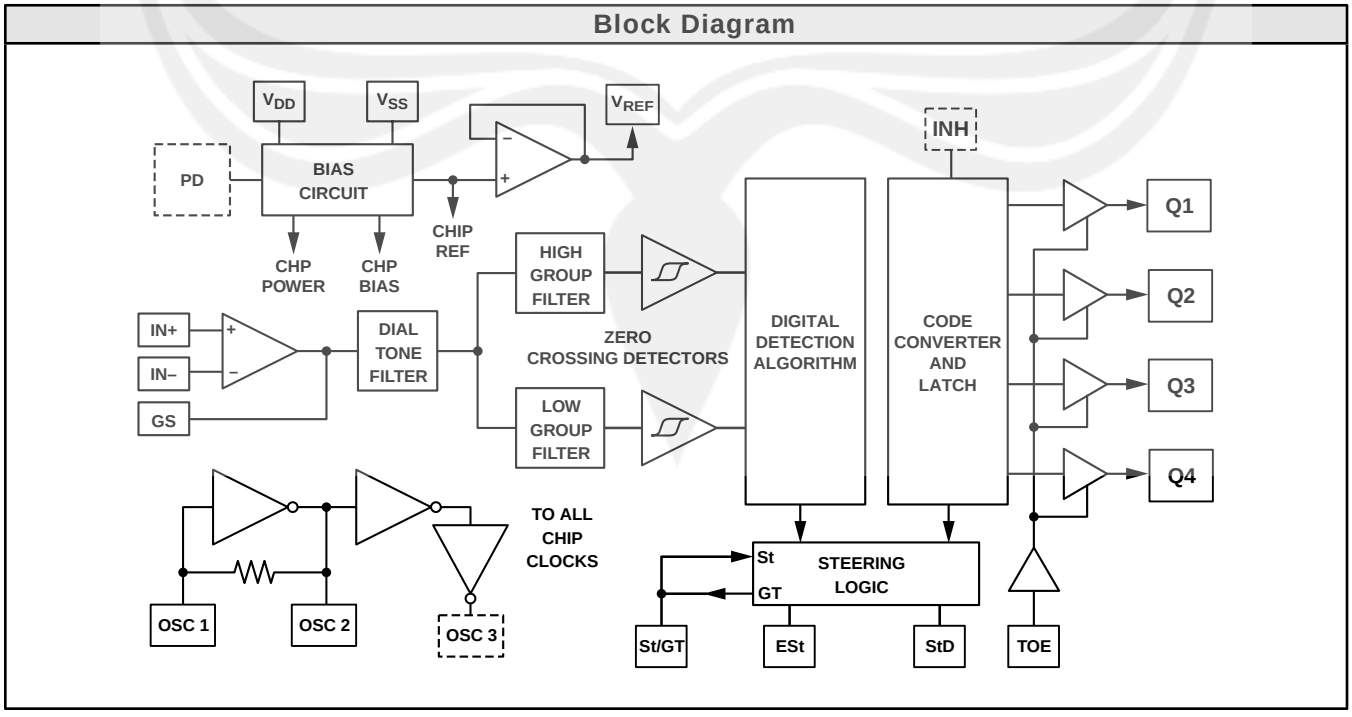
Applications

- PABX
- Central office
- Mobile radio
- Remote control
- Remote data entry
- Call limiting
- Telephone answering systems
- Paging systems

Product Description

The CAMD CM8870/70C provides full DTMF receiver capability by integrating both the band-split filter and digital decoder functions into a single 18-pin DIP, SOIC, or 20-pin PLCC package. The CM8870/70C is manufactured using state-of-the-art CMOS process technology for low power consumption (35mW, MAX) and precise data handling. The filter section uses a switched capacitor technique for both high and low group filters and dial tone rejection. The CM8870/70C decoder uses digital counting techniques for the detection and decoding of all 16 DTMF tone pairs into a 4-bit code. This DTMF receiver minimizes external component count by providing an on-chip differential input amplifier, clock generator, and a latched three-state interface bus. The on-chip clock generator requires only a low cost TV crystal or ceramic resonator as an external component.

Block Diagram



C1581000

Absolute Maximum Ratings: (Note 1)

Absolute Maximum Ratings		
Symbol	**Parameter**	**Value**
V_{DD}	Power Supply Voltage (V_{DD}/V_{SS})	6V MAX
Vdc	Voltage on any Pin	V_{SS} – 0.3V to V_{DD} + 0.3V
I_{DD}	Current on any Pin	10mA MAX
T_A	Operating Temperature	–40˚C to 85˚C
T_S	Storage Temperature	–65˚C to 150˚C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

Notes:

1. Exceeding these ratings may cause permanent damage, functional operation under these conditions is not implied.

DC Characteristics: All voltages referenced to V_{SS}, V_{DD} = 5V ±5%, T_A = –40°C to 85°C unless otherwise noted.

DC Characteristics							
Symbol	**Parameter**		**Test Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
V_{DD}	Operating Supply Voltage			4.75		5.25	V
I_{DD}	Operating Supply Current				3.0	7.0	mA
I_{DDQ}	Standby Supply Current		PD = V_{DD}			25	µA
P_O	Power Consumption		f = 3.579 MHz; V_{DD} = 5V		15	35	mW
V_{IL}	Low Level Input Voltage		V_{DD} = 5V			1.5	V
V_{IH}	High Level Input Voltage		V_{DD} = 5V	3.5			V
I_{IH}/L_{IL}	Input Leakage Current		V_{IN} = V_{SS} = V_{DD} (Note 1)		0.1		µA
I_{SO}	Pull Up (Source) Current on TOE		TOE = 0V, V_{DD} = 5V		6.5	20	µA
R_{IN}	Input Impedance, (IN+, IN–)		@ 1KHz	8	10		MΩ
V_{Tst}	Steering Threshold Voltage		V_{DD} = 5V	2.2		2.5	V
V_{OL}	Low Level Output Voltage		V_{DD} = 5V, No Load			0.03	V
V_{OH}	High Level Output Voltage		V_{DD} = 5V, No Load	4.97			V
I_{OL}	Output Low (Sink) Current		V_{OUT} = 0.4V	1.0	2.5		mA
I_{OH}	Output High (Source) Current		V_{OUT} = 4.6V	0.4	0.8		mA
V_{REF}	Output Voltage	V_{REF}	V_{DD} = 5.0V, No Load	2.4		2.7	V
R_{OR}	Output Resistance				10		kΩ

Operating Characteristics: All voltages referenced to V_{SS}, V_{DD} = 5V ±5%, T_A = –40°C to 85°C unless otherwise noted.
Gain Setting Amplifier

Operating Characteristics						
Symbol	**Parameter**	**Test Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
I_{IN}	Input Leakage Current	V_{SS} < V_{IN} < V_{DD}			±100	nA
R_{IN}	Input Resistance		10			MΩ
V_{OS}	Input Offset Voltage				±25	mV
PSRR	Power Supply Rejection	1 KHz (Note 12)	50			dB
CMRR	Common Mode Rejection	–3V < V_{IN} < 3V	40			dB
A_{VOL}	DC Open Loop Voltage Gain		32			dB
fc	Open Loop Unity Gain Bandwidth		0.3			MHz
V_O	Output Voltage Swing	$R_L \geq$ 100 KW to V_{SS}	4			V_{P-P}
C_L	Maximum Capacitive Load (GS)				100	pF
R_L	Maximum Resistive Load (GS)				50	KΩ
Vcm	Common Mode Range (No Load)	No Load	2.5			V_{P-P}

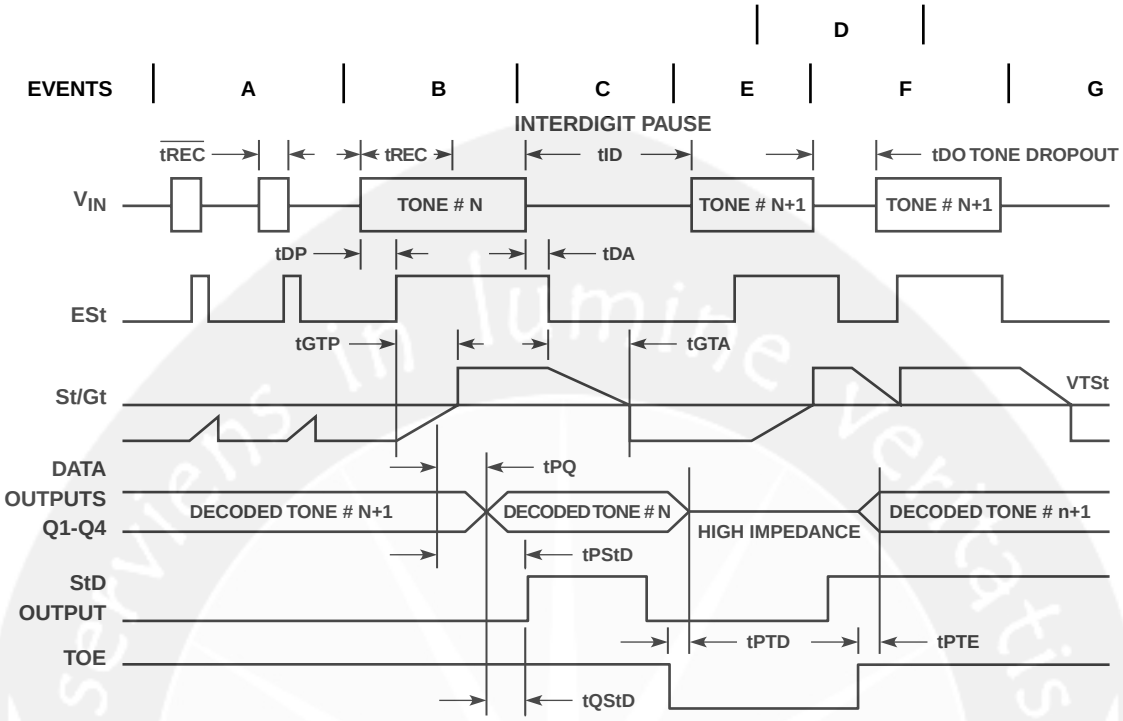
AC Characteristics: All voltages referenced to V_{SS}, V_{DD} = 5.0V ±5%, T_A = –40°C to +85°C, f_{CLK} = 3.579545 MHz using test circuit in Figure 1 unless otherwise noted.

AC Characteristics						
Symbol	**Parameter**	**Notes**	**MIN**	**TYP**	**MAX**	**UNIT**
	Valid Input Signal Levels (each tone of composite signal)	1, 2, 3, 4, 5, 8	–29		1	dBm
			27.5		869	mV_{RMS}
	Positive Twist Accept	2, 3, 4, 8			10	dB
	Negative Twist Accept				10	dB
	Freq. Deviation Aceept Limit	2, 3, 5, 8, 10			1.5%±2Hz	Norm.
	Freq. Deviation Reject Limit	2, 3, 5	±3.5%			Norm.
	Third Tone Tolerance	2, 3, 4, 5, 8, 9, 13, 14		–16		dB
	Noise Tolerance	2, 3, 4, 5, 6, 8, 9		–12		dB
	Dial Tone Tolerance	2, 3, 4,5, 7, 8, 9		22		dB
t_{DP}	Tone Present Detection Time	Refer to Timing Diagram	5	8	14	ms
t_{DA}	Tone Absent Dectection Time	Refer to Timing Diagram	0.5	3	8.5	ms
t_{REC}	MIN Tone Duration Accept	15			40	ms
	MAX Tone Duration Reject	15	20			ms
t_{ID}	MIN Interdigit Pause Accept	15			40	ms
t_{DO}	MAX Interdigit Pause Reject	15	20			µs
t_{PQ}	Propagation Delay (St to Q)	TOE = V_{DD}		6	11	µs
$t_{PS}t_D$	Propagation Delay (St to StD)	TOE = V_{DD}		9	16	µs
$t_{QS}t_D$	Output Data Set Up (Q to StD)	TOE = V_{DD}		3.4		µs
t_{PTE}	Propagation Delay (TOE to Q) Enable	R_L = 10KΩ		50		ns
t_{PTD}	Propagation Delay (TOE to Q) Disable	C_L = 50pf		300		ns
f_{CLK}	Crystal/Clock Frequency		3.5759	3.5795	3.5831	MHz
C_{LO}	Clock Ouput (OSC 2) Capacitive Load				30	pF

Notes:

1. dBm = decibels above or below a reference power of 1mW into a 600Ω load.
2. Digit sequence consists of all 16 DTMF tones.
3. Tone duration = 40ms. Tone pause = 40ms.
4. Nominal DTMF frequencies are used.
5. Both tones in the composite signal have an equal amplitude.
6. Bandwidth limited (0 to 3KHz) Gaussian Noise.
7. The precise dial tone frequencies are (350Hz and 440Hz) ±2%.
8. For an error rate of better than 1 in 10,000
9. Referenced to lowest level frequency component in DTMF signal.
10. Minimum signal acceptance level is measured with specified maximum frequency deviation.
11. Input pins defined as IN+, IN–, and TOE.
12. External voltage source used to bias V_{REF}.
13. This parameter also applies to a third tone injected onto the power supply.
14. Referenced to Figure 1. Input DTMF tone level at –28dBm.
15. Times shown are obtained with circuit in Figure 1 (User adjustable).

Timing Diagram



Explanation of Events

A. Tone bursts detected, tone duration invalid, outputs not updated.

B. Tone #n detected, tone duration valid, tone decoded and latched in outputs.

C. End of tone #n detected, tone absent duration valid, outputs remain latched until next valid tone.

D. Outputs switched to high impedance state.

E. Tone #n + 1 detected, tone duration valid, tone decoded and latched in outputs (currently high impedance).

F. Acceptable dropout of tone #n + 1, tone absent duration invalid, outputs remain latched.

G. End of tone #n + 1 detected, tone absent duration valid, outputs remain latched until next valid tone.

Explanation of Symbols

V_{IN}	DTMF composite input signal.
ESt	Early Steering Output. Indicates detection of valid tone frequencies.
St/GT	Steering input/guard time output. Drives external RC timing circuit.
Q1-Q4	4-bit decoded tone output.
StD	Delayed Steering Output. Indicates that valid frequencies have been present/absent for the required guard time, thus constituting a valid signal.
TOE	Tone Output Enable (input). A low level shifts Q1-Q4 to its high impedance state.
t_{REC}	Maximum DTMF signal duration not detected as valid.
t_{REC}	Minimum DTMF signal duration required for valid recognition.
t_{ID}	Minimum time between valid DTMF signals.
t_{DO}	Maximum allowable drop-out during valid DTMF signal.
t_{DP}	Time to detect the presence of valid DTMF signals.
t_{DA}	Time to detect the absence of valid DTMF signals.
t_{GTP}	Guard time, tone present.
t_{GTA}	Guard time, tone absent.

Functional Description

The CAMD CM8870/70C DTMF Integrated Receiver provides the design engineer with not only low power consumption, but high performance in a small 18-pin DIP, SOIC, or 20-pin PLCC package configuration. The CM8870/70C's internal architecture consists of a band-split filter section which separates the high and low tones of the received pair, followed by a digital decode (counting) section which verifies both the frequency and duration of the received tones before passing the resultant 4-bit code to the output bus.

Filter Section

Separation of the low-group and high-group tones is achieved by applying the dual-tone signal to the inputs of two 9th-order switched capacitor bandpass filters. The bandwidths of these filters correspond to the bands enclosing the low-group and high-group tones (See Figure 3). The filter section also incorporates notches at 350Hz and 440Hz which provides excellent dial tone rejection. Each filter output is followed by a single order switched capacitor section which smooths the signals prior to limiting. Signal limiting is performed by high-gain comparators. These comparators are provided with a hysteresis to prevent detection of unwanted low-level signals and noise. The outputs of the comparators provide full-rail logic swings at the frequencies of the incoming tones.

Decoder Section

The CM8870/70C decoder uses a digital counting technique to determine the frequencies of the limited tones and to verify that these tones correspond to standard DTMF frequencies. A complex averaging algorithm is used to protect against tone simulation by extraneous signals (such as voice) while providing tolerance to small frequency variations. The averaging algorithm has been developed to ensure an optimum combination of immunity to "talk-off" and tolerance to the presence of interfering signals (third tones) and noise. When the detector recognizes the simultaneous presence of two valid tones (known as "signal condition"), it raises the "Early Steering" flag (ESt). Any subsequent loss of signal condition will cause ESt to fall.

Steering Circuit

Before the registration of a decoded tone pair, the receiver checks for a valid signal duration (referred to as "character-recognition-condition"). This check is performed by an external RC time constant driven by E_{St}. A logic high on ESt causes V_C (See Figure 4) to rise as the capacitor discharges. Providing signal condition is maintained (ESt remains high) for the validation period (t_{GTP}), V_C reaches the threshold (V_{TSt}) of the steering logic to register the tone pair, thus latching its corresponding 4-bit code (See Figure 2) into the output latch. At this point, the GT output is activated and drives VC to V_{DD}. GT continues to drive high as long as ESt remains high, signaling that a received tone pair has been registered. The contents of the output latch are made available on the 4-bit output bus by raising the three-state control input (TOE) to a logic high. The steering circuit works in reverse to validate the interdigit pause between signals. Thus, as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions (drop outs) too short to be considered a valid pause. This capability together with the capability of selecting the steering time constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

Guard Time Adjustment

In situations which do not require independent selection of receive and pause, the simple steering circuit of Figure 4 is applicable. Component values are chosen according to the following formula:

$$t_{REC} = t_{DP} + t_{GTP}$$
$$t_{GTP} = 0.67\ RC$$

The value of t_{DP} is a parameter of the device and t_{REC} is the minimum signal duration to be recognized by the receiver. A value for C of 0.1µF is recommended for most applications, leaving R to be selected by the designer. For example, a suitable value of R for a t_{REC} of 40ms would be 300K. A typical circuit using this steering configuration is shown in Figure 1. The timing requirements for most telecommunication applications are satisfied with this circuit. Different steering arrangements may be used to select independently the guard-times for tone-present (t_{GTP}) and tone absent (t_{GTA}). This may be necessary to meet system specifications which place both accept and reject limits on both tone duration and interdigit pause.

Guard time adjustment also allows the designer to tailor system parameters such as talk-off and noise immunity. Increasing t_{REC} improves talk-off performance, since it reduces the probability that tones simulated by speech will maintain signal condition for long enough to be registered. On the other hand, a relatively short t_{REC} with a long t_{DO} would be appropriate for extremely noisy environments where fast acquisition time and immunity to drop-outs would be requirements. Design information for guard time adjustment is shown in Figure 5.

Input Configuration

The input arrangement of the CM8870/70C provides a differential input operational amplifier as well as a bias source (V_{REF}) which is used to bias the inputs at mid-rail.

Provision is made for connection of a feedback resistor to the op-amp output (GS) for adjustment of gain.

In a single-ended configuration, the input pins are connected as shown in Figure 1, with the op-amp connected for unity gain and VREF biasing the input at ½ V_{DD}. Figure 6 shows the differential configuration, which permits the adjustment of gain with the feedback resistor R5.

Clock Circuit

The internal clock circuit is completed with the addition of a standard television color burst crystal or ceramic resonator having a resonant frequency of 3.579545MHz. The CM8870C in a PLCC package has a buffered oscillator output (OSC3) that can be used to drive clock inputs of other devices such as a microprocessor or other CM887X's as shown in Figure 7. Multiple CM8870/70Cs can be connected as shown in figure 8 such that only one crystal or resonator is required.

Pin Function

Name	Function	Discription
IN+	Non-inverting input	Connection to the front-end differential amplifier
IN–	Inverting input	Connection to the front-end differential amplifier
GS	Gain select	Gives access to output of front-end differential amplifier for connection of feedback resistor.
V_{REF}	Reference output Voltage (nominally $V_{DD}/2$)	May be used to bias the inputs at mid-rail.
INH	Inhibits detection of tones	Represents keys A, B, C, and D
OSC3	Digital buffered oscillator output	
PD	Power down	Logic high powers down the device and inhibits the oscillator.
OSC1	Clock input	3.579545MHz crystal connected between these pins completes internal oscillator
OSC2	Clock output	3.579545MHz crystal connected between these pins completes internal oscillator
V_{SS}	Negative power supply	Normally connected to OV
TOE	Three-state output enable (Input)	Logic high enables the outputs Q1-Q4. Internal pull-up.
Q_1 Q_2 Q_3 Q_4	Three-state ouputs	When enabled by TOE, provides the code corresponding to the last valid tone pair received. (See Figure 2).
StD	Delayed Steering output	Presents a logic high when a received tone pair has been registered and the output latch is updated. Returns to logic low shen the voltage on St/GT falls below V_{TSt}.
ESt	Early steering output	Presents logic high immediately when the digital algorithm detects a recongnizable tone pair (signal condition). Any momentary loss of signal condition will cause ESt to return to a logic low.
St/Gt	Steering input/guard time output (bidirectional)	A voltage greater than V_{TSt} detected at St causes the device to register the dectected tone pair. The GT output acts to reset the external steering time constrant, and its state is a function of ESt and the voltage on St. (See Figure 2).
V_{DD}	Positve power supply	
IC	Internal connection	Must be tied to V_{SS} (for 8870 configuration only).

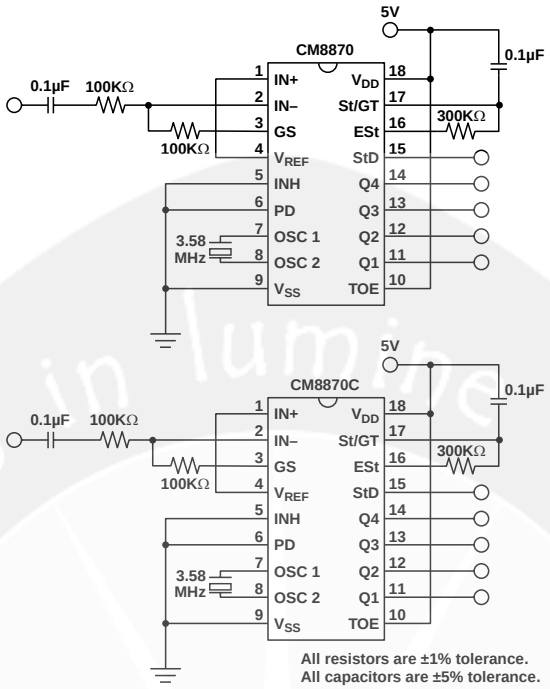
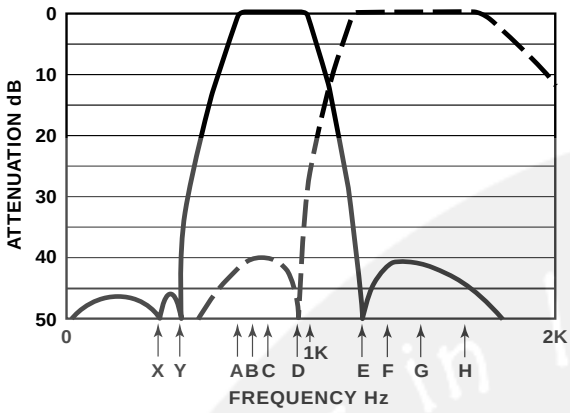


Figure 1. Single Ended Input Configuration

Functional Diode Table							
F_{LOW}	F_{HIGH}	KEY	TOW	Q_4	Q_3	Q_2	Q_1
697	1209	1	H	0	0	0	1
697	1336	2	H	0	0	1	0
697	1477	3	H	0	0	1	1
770	1209	4	H	0	1	0	0
770	1336	5	H	0	1	0	1
770	1477	6	H	0	1	1	0
852	1209	7	H	0	1	1	1
852	1336	8	H	1	0	0	0
852	1477	9	H	1	0	0	1
941	1336	0	H	1	0	1	0
941	1209	*	H	1	0	1	1
941	1477	#	H	1	1	0	0
697	1633	A	H	1	1	0	1
770	1633	B	H	1	1	1	0
852	1633	C	H	1	1	1	1
941	1633	D	H	0	0	0	0
-	-	ANY	L	Z	Z	Z	Z
L Logic Low, H = Logic, Z = High Impedance							

Figure 2. Functional Decode Table



PRECISE DIAL TONES

X = 350Hz
y = 440Hz

DTMF TONES

A = 607Hz	E = 1209Hz
B = 770Hz	F = 1336Hz
C = 852Hz	G = 1477Hz
D = 841Hz	H = 1633Hz

Figure 3. Typical Filter Characteristic

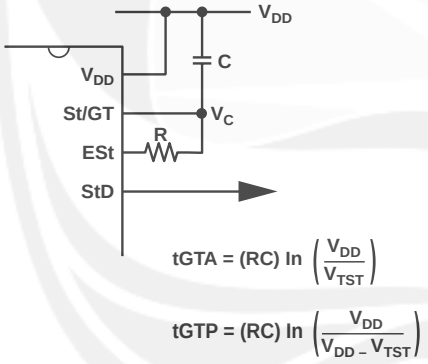


Figure 4. Basic Steering Circuit

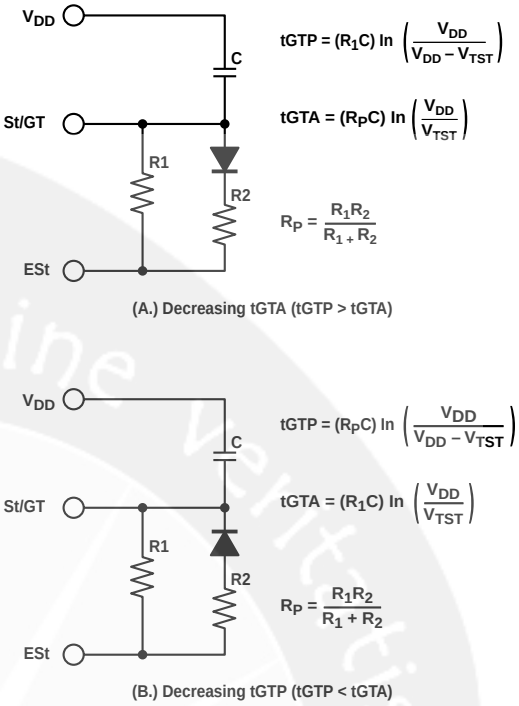
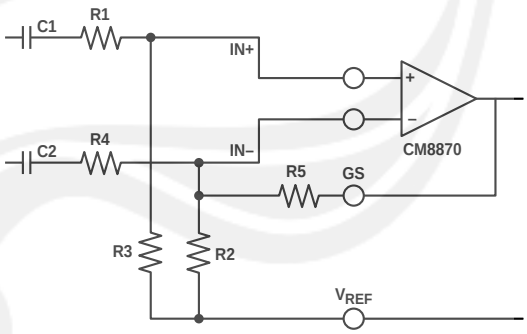


Figure 5. Guard Time Adjustment



All resistors are –1% tolerance.
All capacitors are –5% tolerance.

DIFFERENTIAL INPUT AMPLIFIER

C1 = C2 = 10nF
R1 = R4 = R4 =100 KΩ
R2 = 60KΩ, R3 = 37.5KΩ

$R3 = \frac{R2R5}{R2 + R5}$

VOLTAGE GAIN (Av diff) = $\frac{R5}{R1}$

IMPUT IMPEDANCE

$(Xxxx) = 2\sqrt{R2 + \left(\frac{1}{wC}\right)^2}$

Figure 6. Differential Input Configuration

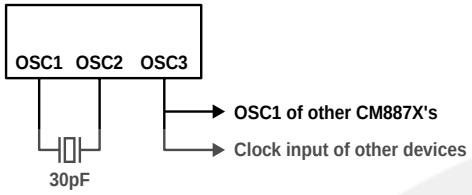


Figure 7. CM8870C Crystal Connection (PLCC Package Only)

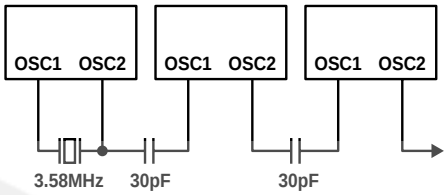
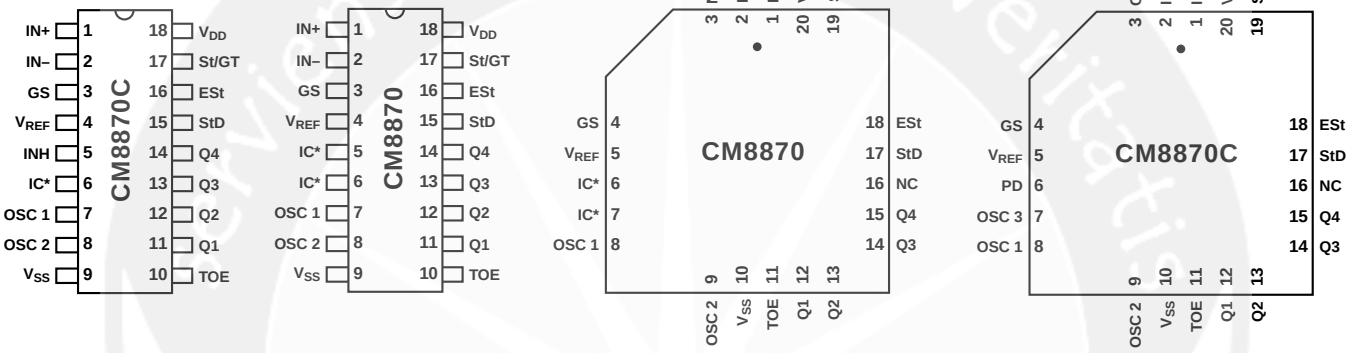


Figure 8. CM8870/70C Crystal Connection

Pin Assignments



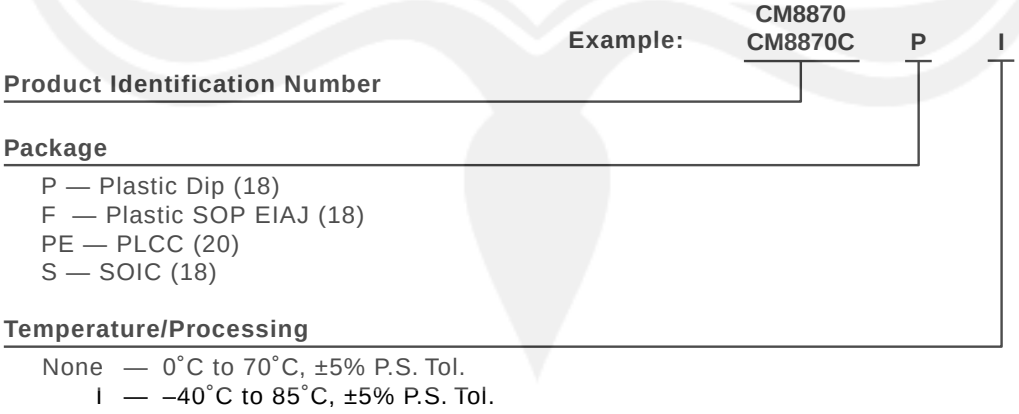
P – Plastic DIP (18)
F – Plastic SOP EIAJ (18)
S – SPIC (18)

P – Plastic DIP (18)
F – Plastic SOP EIAJ (18)
S – SOIC (18)

PE – PLCC (20)
* – Connected to V_{SS}

PE – PLCC (20)

Ordering Information



GlobalOptoisolator™

VDE	UL	CSA	SETI	SEMKO	DEMKO	NEMKO	BABT

6-Pin DIP Optoisolators Transistor Output

4N25*
4N25A*
4N26*
[CTR = 20% Min]
4N27
4N28
[CTR = 10% Min]

*Motorola Preferred Devices

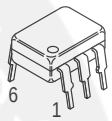
The 4N25/A, 4N26, 4N27 and 4N28 devices consist of a gallium arsenide infrared emitting diode optically coupled to a monolithic silicon phototransistor detector.

- Most Economical Optoisolator Choice for Medium Speed, Switching Applications
- Meets or Exceeds All JEDEC Registered Specifications
- ***To order devices that are tested and marked per VDE 0884 requirements, the suffix "V" must be included at end of part number. VDE 0884 is a test option.***

Applications

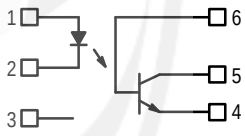
- General Purpose Switching Circuits
- Interfacing and coupling systems of different potentials and impedances
- I/O Interfacing
- Solid State Relays

STYLE 1 PLASTIC



STANDARD THRU HOLE
CASE 730A–04

SCHEMATIC



PIN 1. LED ANODE
2. LED CATHODE
3. N.C.
4. EMITTER
5. COLLECTOR
6. BASE

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
INPUT LED			
Reverse Voltage	V_R	3	Volts
Forward Current — Continuous	I_F	60	mA
LED Power Dissipation @ T_A = 25°C with Negligible Power in Output Detector Derate above 25°C	P_D	120 1.41	mW mW/°C
OUTPUT TRANSISTOR			
Collector–Emitter Voltage	V_{CEO}	30	Volts
Emitter–Collector Voltage	V_{ECO}	7	Volts
Collector–Base Voltage	V_{CBO}	70	Volts
Collector Current — Continuous	I_C	150	mA
Detector Power Dissipation @ T_A = 25°C with Negligible Power in Input LED Derate above 25°C	P_D	150 1.76	mW mW/°C
TOTAL DEVICE			
Isolation Surge Voltage(1) (Peak ac Voltage, 60 Hz, 1 sec Duration)	V_{ISO}	7500	Vac(pk)
Total Device Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	250 2.94	mW mW/°C
Ambient Operating Temperature Range(2)	T_A	–55 to +100	°C
Storage Temperature Range(2)	T_{stg}	–55 to +150	°C
Soldering Temperature (10 sec, 1/16″ from case)	T_L	260	°C

1. Isolation surge voltage is an internal device dielectric breakdown rating. For this test, Pins 1 and 2 are common, and Pins 4, 5 and 6 are common.
2. Refer to Quality and Reliability Section in Opto Data Book for information on test conditions.

Preferred devices are Motorola recommended choices for future use and best overall value.
GlobalOptoisolator is a trademark of Motorola, Inc.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)(1)

Characteristic		Symbol	Min	Typ(1)	Max	Unit
INPUT LED						
Forward Voltage (I_F = 10 mA)	T_A = 25°C T_A = –55°C T_A = 100°C	V_F	— — —	1.15 1.3 1.05	1.5 — —	Volts
Reverse Leakage Current (V_R = 3 V)		I_R	—	—	100	µA
Capacitance (V = 0 V, f = 1 MHz)		C_J	—	18	—	pF
OUTPUT TRANSISTOR						
Collector–Emitter Dark Current (V_{CE} = 10 V, T_A = 25°C	4N25,25A,26,27 4N28	I_{CEO}	— —	1 1	50 100	nA
(V_{CE} = 10 V, T_A = 100°C)	All Devices	I_{CEO}	—	1	—	µA
Collector–Base Dark Current (V_{CB} = 10 V)		I_{CBO}	—	0.2	—	nA
Collector–Emitter Breakdown Voltage (I_C = 1 mA)		$V_{(BR)CEO}$	30	45	—	Volts
Collector–Base Breakdown Voltage (I_C = 100 µA)		$V_{(BR)CBO}$	70	100	—	Volts
Emitter–Collector Breakdown Voltage (I_E = 100 µA)		$V_{(BR)ECO}$	7	7.8	—	Volts
DC Current Gain (I_C = 2 mA, V_{CE} = 5 V)		h_{FE}	—	500	—	—
Collector–Emitter Capacitance (f = 1 MHz, V_{CE} = 0)		C_{CE}	—	7	—	pF
Collector–Base Capacitance (f = 1 MHz, V_{CB} = 0)		C_{CB}	—	19	—	pF
Emitter–Base Capacitance (f = 1 MHz, V_{EB} = 0)		C_{EB}	—	9	—	pF
COUPLED						
Output Collector Current (I_F = 10 mA, V_{CE} = 10 V)	4N25,25A,26 4N27,28	I_C (CTR)(2)	2 (20) 1 (10)	7 (70) 5 (50)	— —	mA (%)
Collector–Emitter Saturation Voltage (I_C = 2 mA, I_F = 50 mA)		$V_{CE(sat)}$	—	0.15	0.5	Volts
Turn–On Time (I_F = 10 mA, V_{CC} = 10 V, R_L = 100 Ω)(3)		t_{on}	—	2.8	—	µs
Turn–Off Time (I_F = 10 mA, V_{CC} = 10 V, R_L = 100 Ω)(3)		t_{off}	—	4.5	—	µs
Rise Time (I_F = 10 mA, V_{CC} = 10 V, R_L = 100 Ω)(3)		t_r	—	1.2	—	µs
Fall Time (I_F = 10 mA, V_{CC} = 10 V, R_L = 100 Ω)(3)		t_f	—	1.3	—	µs
Isolation Voltage (f = 60 Hz, t = 1 sec)(4)		V_{ISO}	7500	—	—	Vac(pk)
Isolation Resistance (V = 500 V)(4)		R_{ISO}	10^{11}	—	—	Ω
Isolation Capacitance (V = 0 V, f = 1 MHz)(4)		C_{ISO}	—	0.2	—	pF

1. Always design to the specified minimum/maximum electrical limits (where applicable).
2. Current Transfer Ratio (CTR) = I_C/I_F x 100%.
3. For test circuit setup and waveforms, refer to Figure 11.
4. For this test, Pins 1 and 2 are common, and Pins 4, 5 and 6 are common.

TYPICAL CHARACTERISTICS

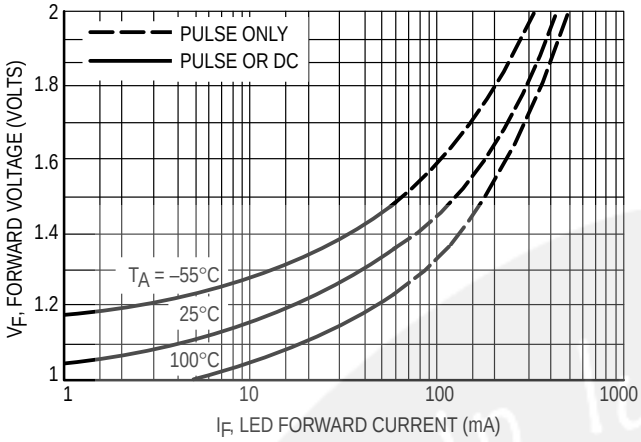


Figure 1. LED Forward Voltage versus Forward Current

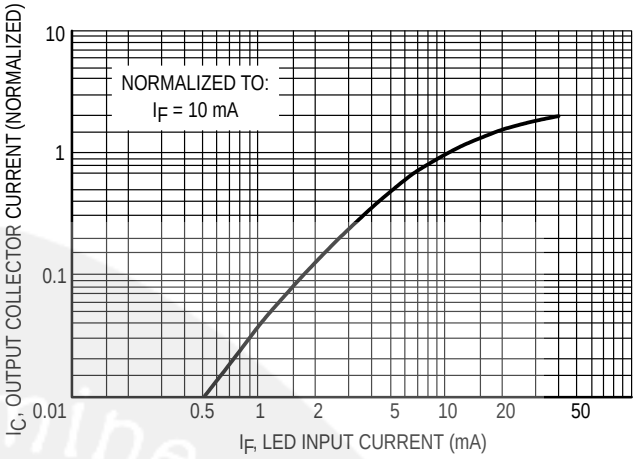


Figure 2. Output Current versus Input Current

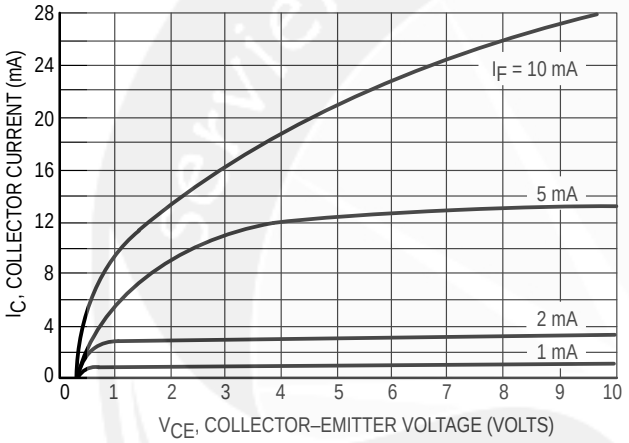


Figure 3. Collector Current versus Collector–Emitter Voltage

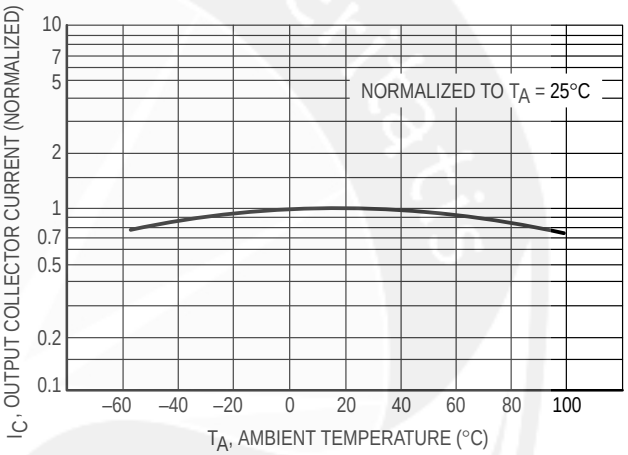


Figure 4. Output Current versus Ambient Temperature

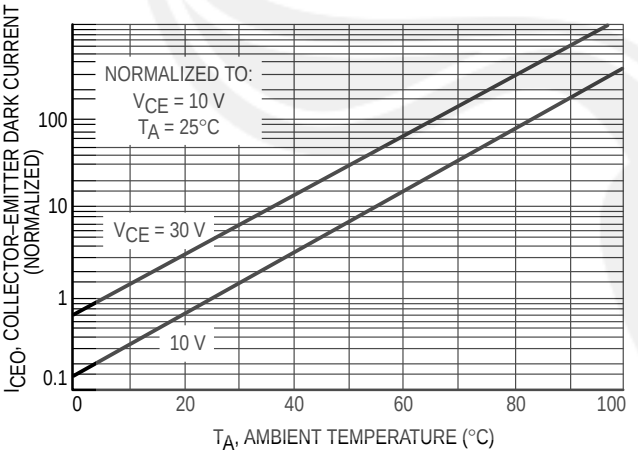


Figure 5. Dark Current versus Ambient Temperature

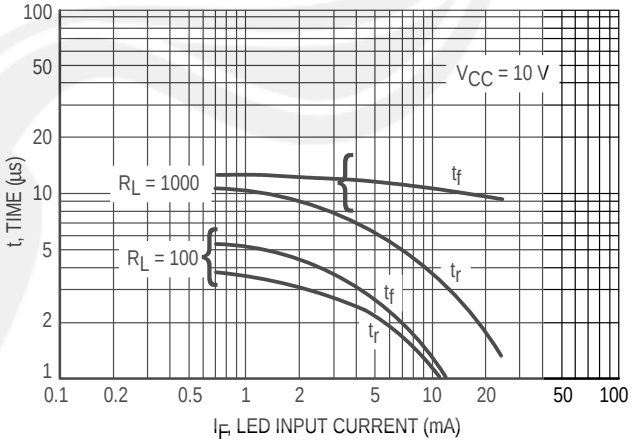


Figure 6. Rise and Fall Times (Typical Values)

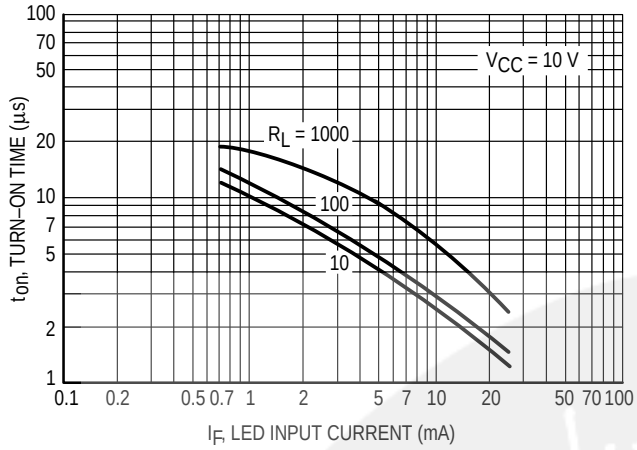


Figure 7. Turn–On Switching Times (Typical Values)

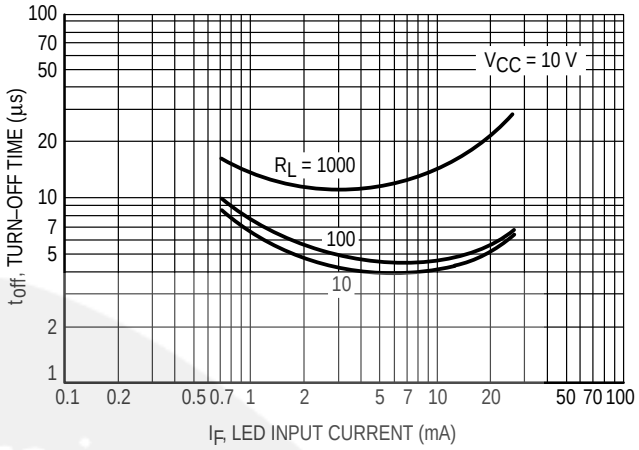


Figure 8. Turn–Off Switching Times (Typical Values)

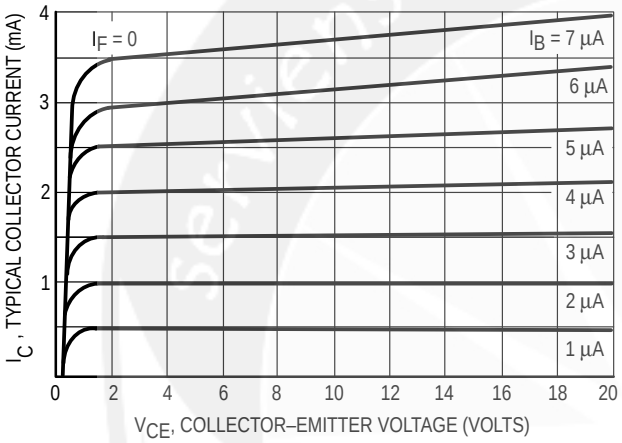


Figure 9. DC Current Gain (Detector Only)

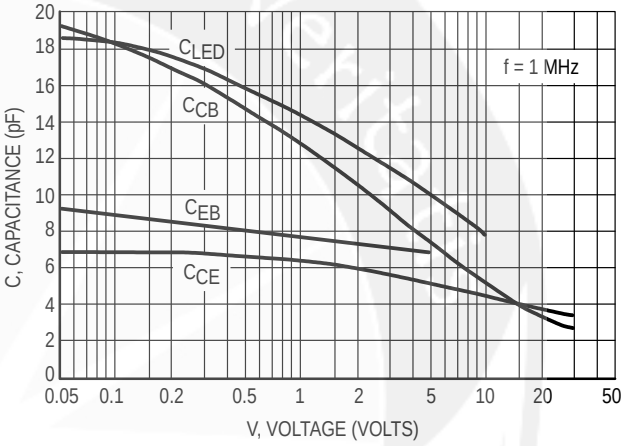


Figure 10. Capacitances versus Voltage

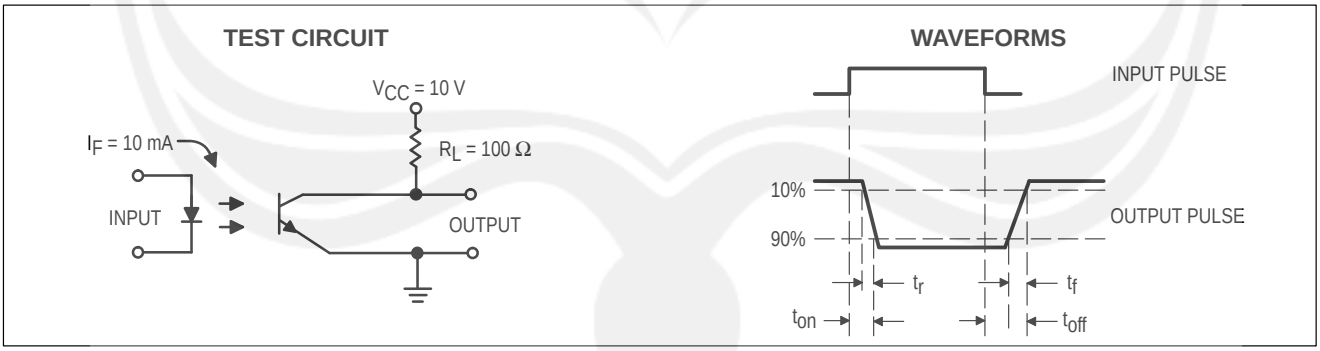
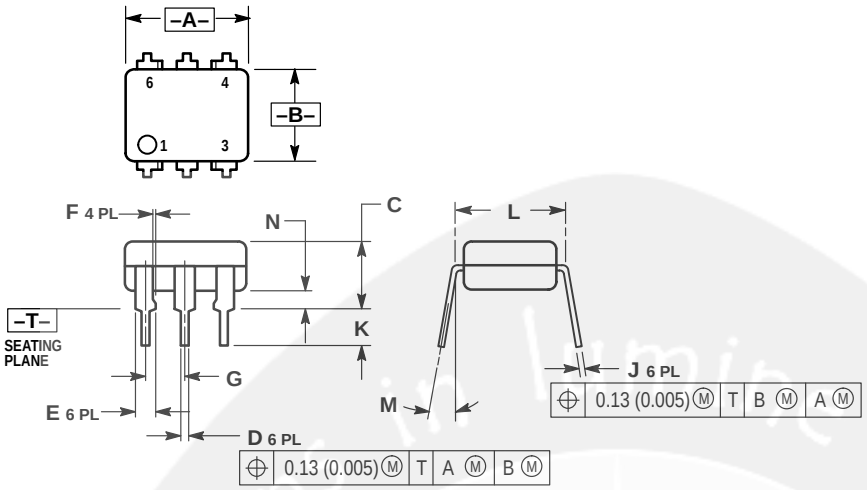


Figure 11. Switching Time Test Circuit and Waveforms

PACKAGE DIMENSIONS

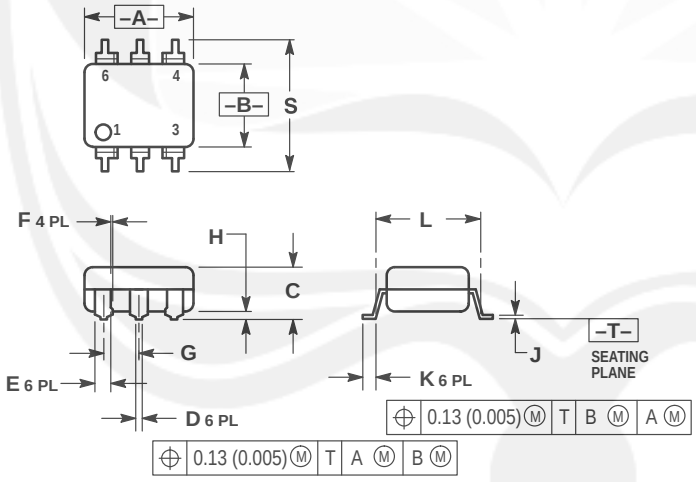


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.320	0.350	8.13	8.89
B	0.240	0.260	6.10	6.60
C	0.115	0.200	2.93	5.08
D	0.016	0.020	0.41	0.50
E	0.040	0.070	1.02	1.77
F	0.010	0.014	0.25	0.36
G	0.100 BSC		2.54 BSC	
J	0.008	0.012	0.21	0.30
K	0.100	0.150	2.54	3.81
L	0.300 BSC		7.62 BSC	
M	0 °	15 °	0 °	15 °
N	0.015	0.100	0.38	2.54

STYLE 1:
PIN 1. ANODE
2. CATHODE
3. NC
4. EMITTER
5. COLLECTOR
6. BASE

CASE 730A–04
ISSUE G



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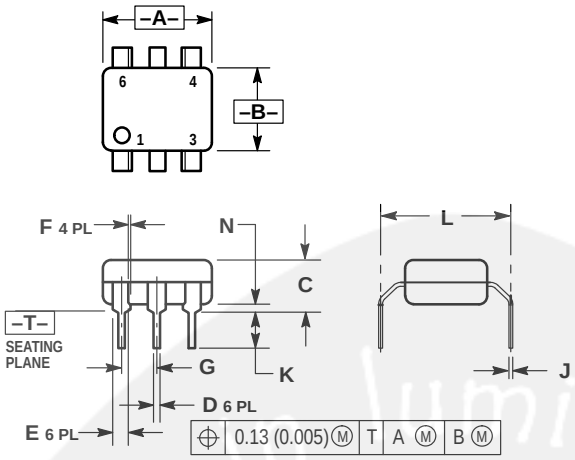
D	0.016	0.020	0.41	0.50
E	0.040	0.070	1.02	1.77
F	0.010	0.014	0.25	0.36
G	0.100 BSC		2.54 BSC	
H	0.020	0.025	0.51	0.63
J	0.008	0.012	0.20	0.30
K	0.006	0.035	0.16	0.88
L	0.320 BSC		8.13 BSC	
S	0.332	0.390	8.43	9.90

***Consult factory for leadform option availability**

CASE 730C–04
ISSUE D



NOTES:
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2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.320	0.350	8.13	8.89
B	0.240	0.260	6.10	6.60
C	0.115	0.200	2.93	5.08
D	0.016	0.020	0.41	0.50
E	0.040	0.070	1.02	1.77
F	0.010	0.014	0.25	0.36
G	0.100 BSC		2.54 BSC	
J	0.008	0.012	0.21	0.30
K	0.100	0.150	2.54	3.81
L	0.400	0.425	10.16	10.80
N	0.015	0.040	0.38	1.02

***Consult factory for leadform option availability**

CASE 730D–05
ISSUE D

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HONG KONG: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298

TLP521GB, TLP521-2GB, TLP521-4GB, TLP521, TLP521-2, TLP521-4
TLP521XGB, TLP521-2XGB, TLP521-4XGB
TLP521X, TLP521-2X, TLP521-4X

HIGH DENSITY MOUNTING PHOTOTRANSISTOR OPTICALLY COUPLED ISOLATORS

APPROVALS

- UL recognised, File No. E91231

'X' SPECIFICATION APPROVALS

- VDE 0884 in 3 available lead form : -
  - STD
  - G form
  - SMD approved to CECC 00802
- BSI approved - Certificate No. 8001

DESCRIPTION

The TLP521, TLP521-2, TLP521-4 series of optically coupled isolators consist of infrared light emitting diodes and NPN silicon photo transistors in space efficient dual in line plastic packages.

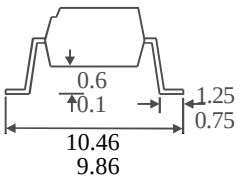
FEATURES

- Options :-
  10mm lead spread - add G after part no.
  Surface mount - add SM after part no.
  Tape&reel - add SMT&R after part no.
- High Current Transfer Ratio (50% min)
- High Isolation Voltage ($5.3kV_{RMS}$, $7.5kV_{PK}$)
- High BV_{CEO} (55Vmin)
- All electrical parameters 100% tested
- Custom electrical selections available

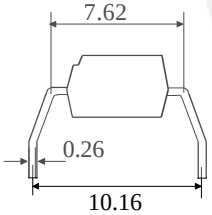
APPLICATIONS

- Computer terminals
- Industrial systems controllers
- Measuring instruments
- Signal transmission between systems of different potentials and impedances

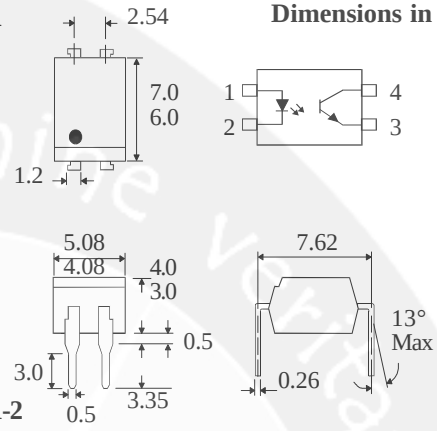
OPTION SM
SURFACE MOUNT



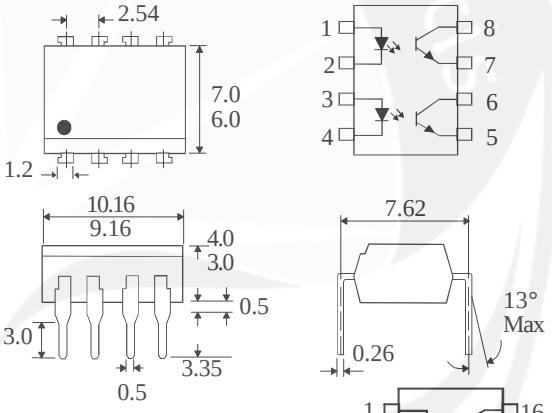
OPTION G



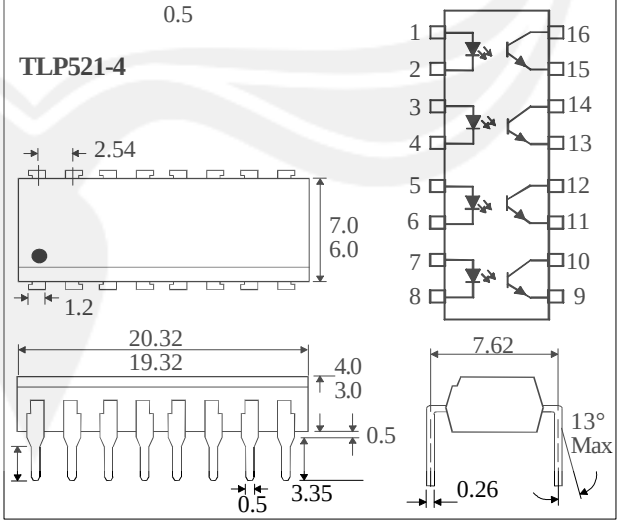
TLP521 **Dimensions in mm**



TLP521-2



TLP521-4



ISOCOM COMPONENTS LTD
Unit 25B, Park View Road West,
Park View Industrial Estate, Brenda Road
Hartlepool, Cleveland, TS25 1YD
Tel: (01429) 863609 Fax :(01429) 863581

ABSOLUTE MAXIMUM RATINGS
(25°C unless otherwise specified)

Storage Temperature	-55°C to + 125°C
Operating Temperature	-30°C to + 100°C
Lead Soldering Temperature (1/16 inch (1.6mm) from case for 10 secs)	260°C

INPUT DIODE

Forward Current	50mA
Reverse Voltage	6V
Power Dissipation	70mW

OUTPUT TRANSISTOR

Collector-emitter Voltage BV_{CEO}	55V
Emitter-collector Voltage BV_{ECO}	6V
Power Dissipation	150mW

POWER DISSIPATION

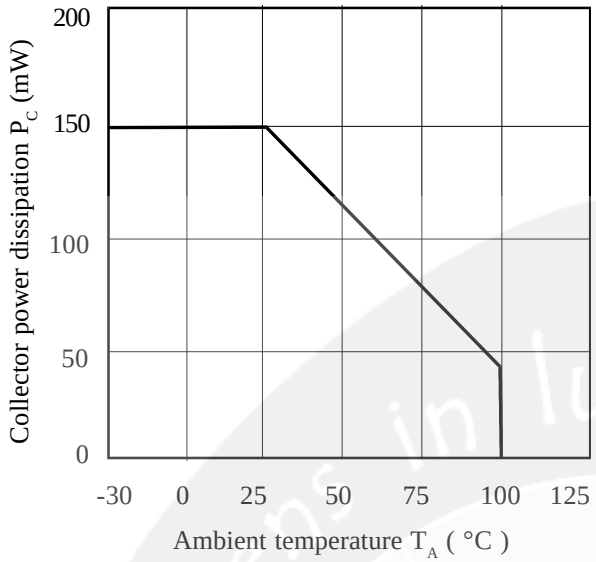
Total Power Dissipation (derate linearly 2.67mW/°C above 25°C)	200mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C Unless otherwise noted)

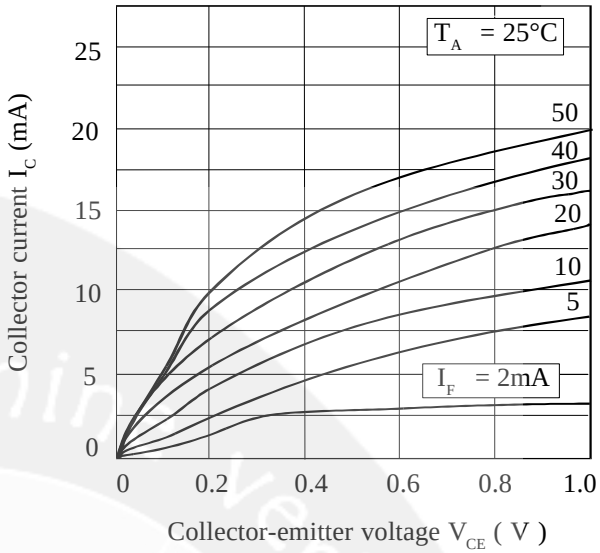
PARAMETER		MIN	TYP	MAX	UNITS	TEST CONDITION
Input	Forward Voltage (V_F)	1.0	1.15	1.3	V	I_F = 10mA
	Reverse Current (I_R)			10	µA	V_R = 4V
Output	Collector-emitter Breakdown (BV_{CEO}) (Note 2)	55			V	I_C = 0.5mA
	Emitter-collector Breakdown (BV_{ECO})	6			V	I_E = 100µA
	Collector-emitter Dark Current (I_{CEO})			100	nA	V_{CE} = 20V
Coupled	Current Transfer Ratio (CTR) (Note 2)					
	TLP521, TLP521-2, TLP521-4	50		600	%	5mA I_F, 5V V_{CE}
	CTR selection available BL	200		600	%	
	GB	100		600	%	
	GB	30			%	1mA I_F, 0.4V V_{CE}
	Collector-emitter Saturation Voltage $V_{CE\ (SAT)}$			0.4	V	8mA I_F, 2.4mA I_C
	-GB			0.4	V	1mA I_F, 0.2mA I_C
	Input to Output Isolation Voltage V_{ISO}	5300			V_{RMS}	See note 1
		7500			V_{PK}	See note 1
	Input-output Isolation Resistance R_{ISO}	$5x10^{10}$			Ω	V_{IO} = 500V (note 1)
	Response Time (Rise), tr		4		µs	V_{CE} = 2V,
	Response Time (Fall), tf		3		µs	I_C = 2mA, R_L = 100Ω

Note 1 Measured with input leads shorted together and output leads shorted together.
Note 2 Special Selections are available on request. Please consult the factory.

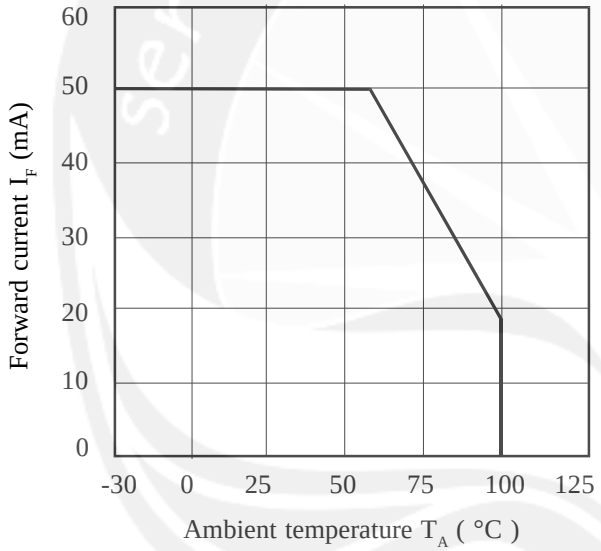
Collector Power Dissipation vs. Ambient Temperature



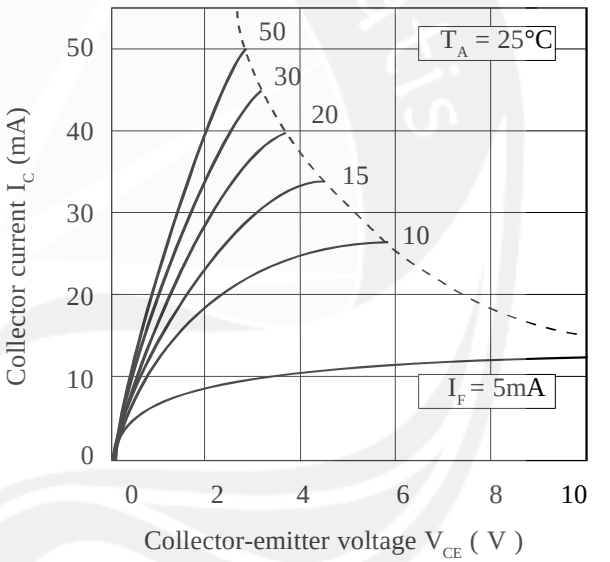
Collector Current vs. Low Collector-emitter Voltage



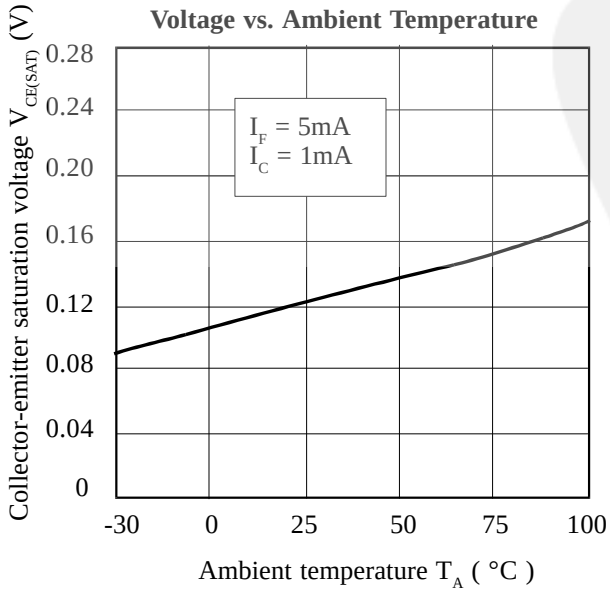
Forward Current vs. Ambient Temperature



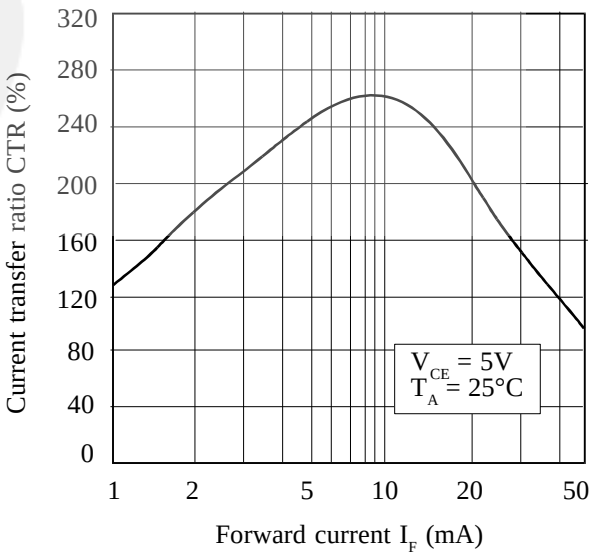
Collector Current vs. Collector-emitter Voltage



Collector-emitter Saturation Voltage vs. Ambient Temperature



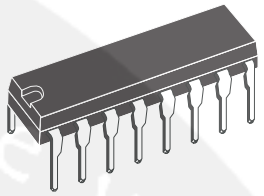
Current Transfer Ratio vs. Forward Current



ULN2001A-ULN2002A
ULN2003A-ULN2004A

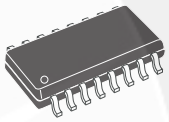
SEVEN DARLINGTON ARRAYS

- SEVEN DARLINGTONS PER PACKAGE
- OUTPUT CURRENT 500mA PER DRIVER (600mA PEAK)
- OUTPUT VOLTAGE 50V
- INTEGRATED SUPPRESSION DIODES FOR INDUCTIVE LOADS
- OUTPUTS CAN BE PARALLELED FOR HIGHER CURRENT
- TTL/CMOS/PMOS/DTL COMPATIBLE INPUTS
- INPUTS PINNED OPPOSITE OUTPUTS TO SIMPLIFY LAYOUT



DIP16

ORDERING NUMBERS: ULN2001A/2A/3A/4A



SO16

ORDERING NUMBERS: ULN2001D/2D/3D/4D

DESCRIPTION

The ULN2001A, ULN2002A, ULN2003 and ULN2004A are high voltage, high current darlington arrays each containing seven open collector darlington pairs with common emitters. Each channel rated at 500mA and can withstand peak currents of 600mA. Suppression diodes are included for inductive load driving and the inputs are pinned opposite the outputs to simplify board layout.

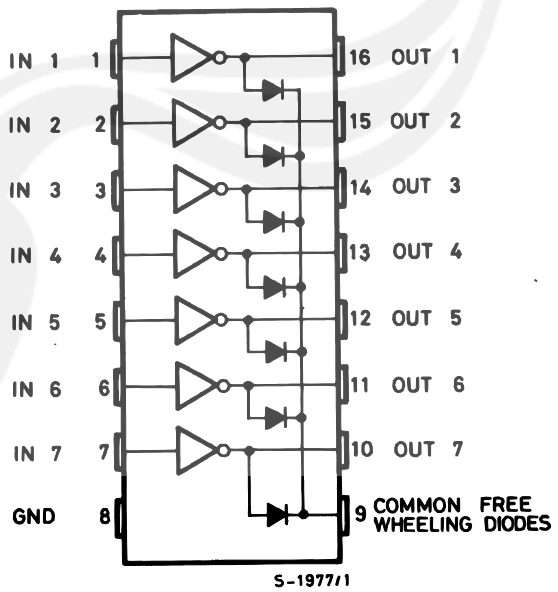
The four versions interface to all common logic families :

ULN2001A	General Purpose, DTL, TTL, PMOS, CMOS
ULN2002A	14-25V PMOS
ULN2003A	5V TTL, CMOS
ULN2004A	6–15V CMOS, PMOS

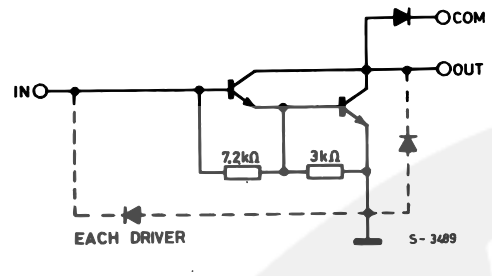
These versatile devices are useful for driving a wide range of loads including solenoids, relays DC motors, LED displays filament lamps, thermal printheads and high power buffers.

The ULN2001A/2002A/2003A and 2004A are supplied in 16 pin plastic DIP packages with a copper leadframe to reduce thermal resistance. They are available also in small outline package (SO-16) as ULN2001D/2002D/2003D/2004D.

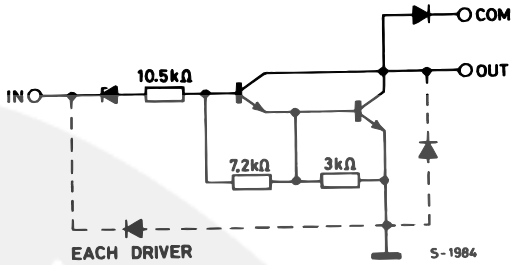
PIN CONNECTION



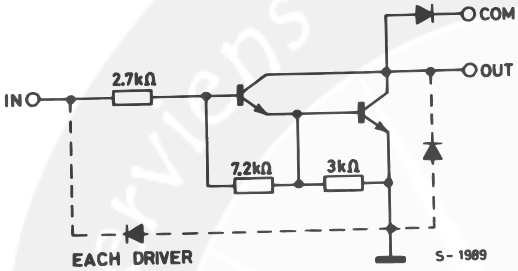
SCHEMATIC DIAGRAM



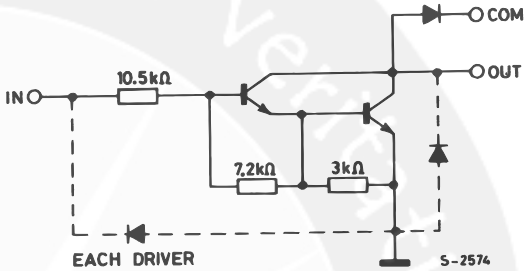
Series ULN-2001A
(each driver)



Series ULN-2002A
(each driver)



Series ULN-2003A
(each driver)



Series ULN-2004A
(each driver)

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_o	Output Voltage	50	V
V_{in}	Input Voltage (for ULN2002A/D - 2003A/D - 2004A/D)	30	V
I_c	Continuous Collector Current	500	mA
I_b	Continuous Base Current	25	mA
T_{amb}	Operating Ambient Temperature Range	– 20 to 85	°C
T_{stg}	Storage Temperature Range	– 55 to 150	°C
T_j	Junction Temperature	150	°C

THERMAL DATA

Symbol	Parameter		DIP16	SO16	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max.	70	120	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_{CEX}	Output Leakage Current	V_{CE} = 50V T_{amb} = 70°C, V_{CE} = 50V T_{amb} = 70°C for ULN2002A V_{CE} = 50V, V_i = 6V for ULN2004A V_{CE} = 50V, V_i = 1V			50 100 500 500	µA µA µA µA	1a 1a 1b 1b
$V_{CE(sat)}$	Collector-emitter Saturation Voltage	I_C = 100mA, I_B = 250µA I_C = 200 mA, I_B = 350µA I_C = 350mA, I_B = 500µA		0.9 1.1 1.3	1.1 1.3 1.6	V V V	2 2 2
$I_{i(on)}$	Input Current	for ULN2002A, V_i = 17V for ULN2003A, V_i = 3.85V for ULN2004A, V_i = 5V V_i = 12V		0.82 0.93 0.35 1	1.25 1.35 0.5 1.45	mA mA mA mA	3 3 3 3
$I_{i(off)}$	Input Current	T_{amb} = 70°C, I_C = 500µA	50	65		µA	4
$V_{i(on)}$	Input Voltage	V_{CE} = 2V for ULN2002A I_C = 300mA for ULN2003A I_C = 200mA I_C = 250mA I_C = 300mA for ULN2004A I_C = 125mA I_C = 200mA I_C = 275mA I_C = 350mA			 13 2.4 2.7 3 5 6 7 8	V	5
h_{FE}	DC Forward Current Gain	for ULN2001A V_{CE} = 2V, I_C = 350mA	1000				2
C_i	Input Capacitance			15	25	pF	
t_{PLH}	Turn-on Delay Time	0.5 V_i to 0.5 V_o		0.25	1	µs	
t_{PHL}	Turn-off Delay Time	0.5 V_i to 0.5 V_o		0.25	1	µs	
I_R	Clamp Diode Leakage Current	V_R = 50V T_{amb} = 70°C, V_R = 50V			50 100	µA µA	6 6
V_F	Clamp Diode Forward Voltage	I_F = 350mA		1.7	2	V	7

TEST CIRCUITS

Figure 1a.

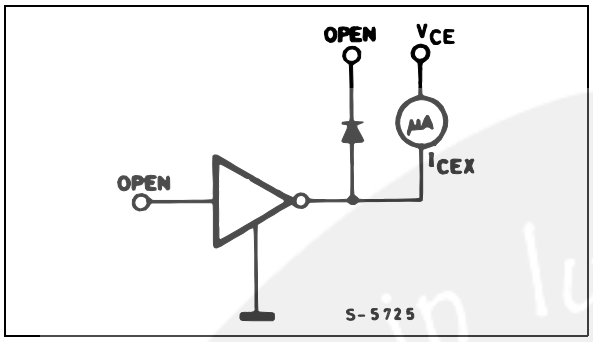


Figure 1b.

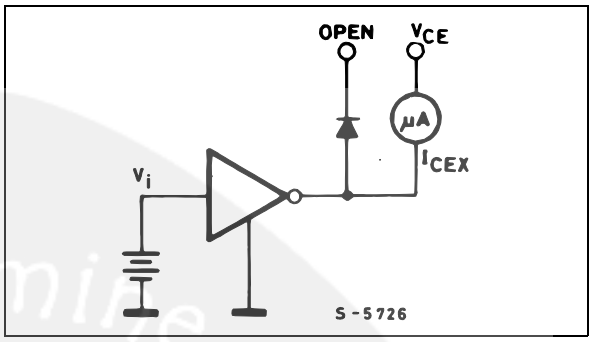


Figure 2.

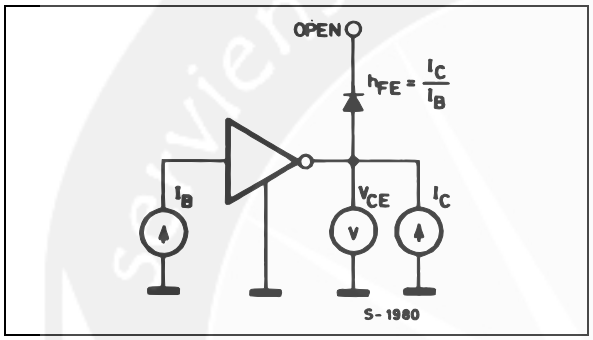


Figure 3.

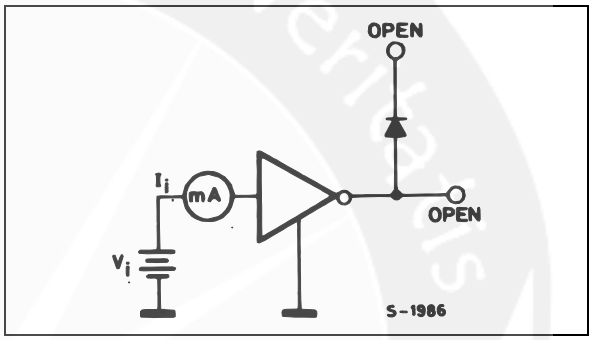


Figure 4.

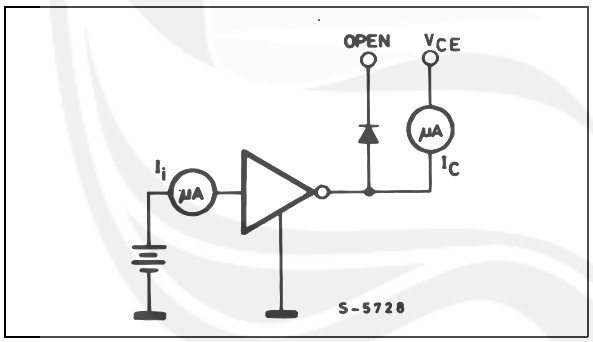


Figure 5.

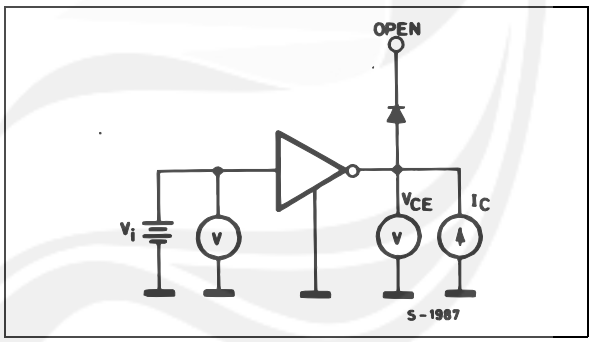


Figure 6.

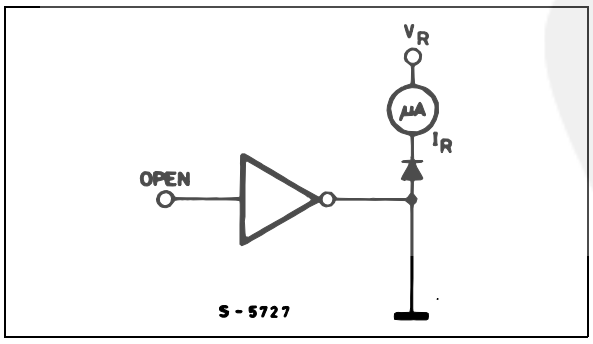


Figure 7.

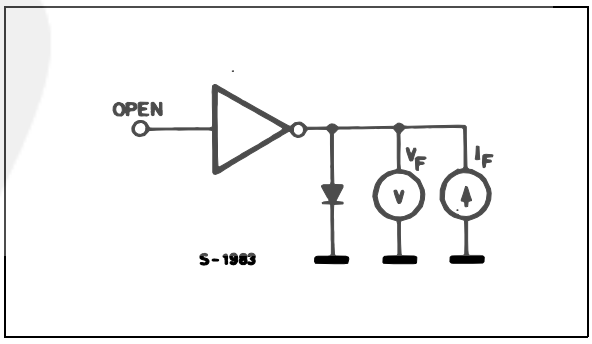


Figure 8: Collector Current versus Input Current

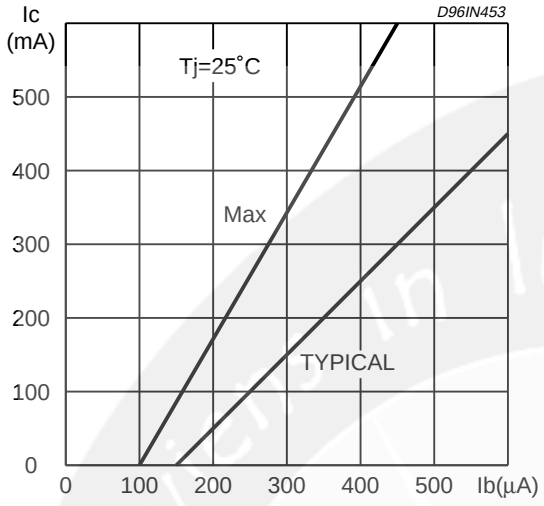


Figure 9: Collector Current versus Saturation Voltage

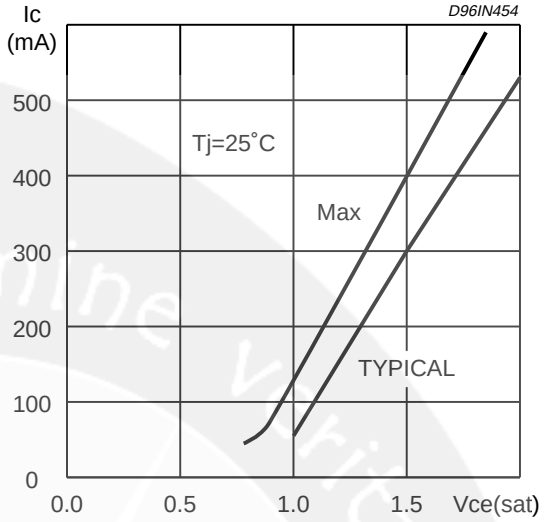


Figure 10: Peak Collector Current versus Duty Cycle

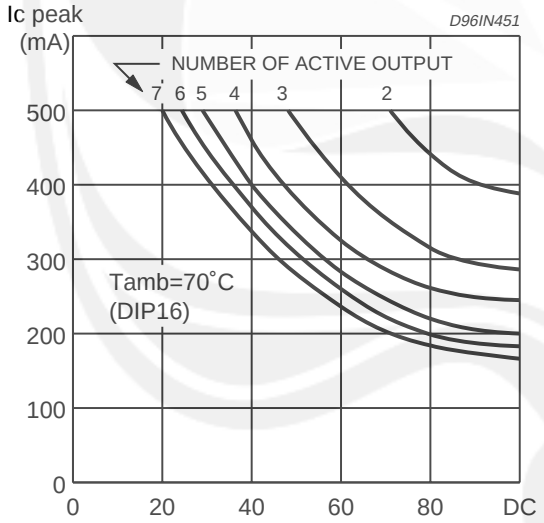
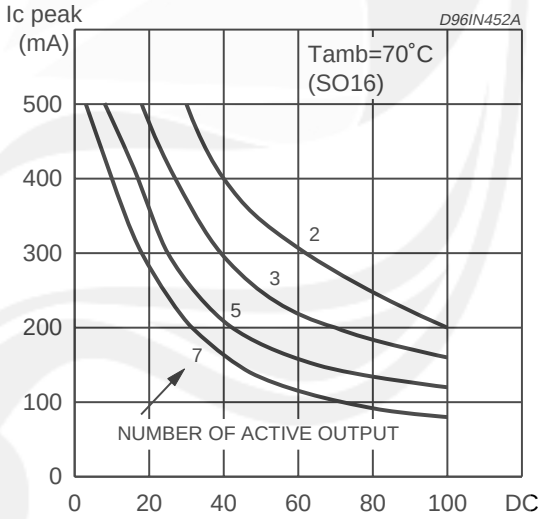
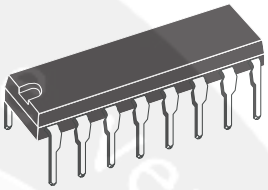


Figure 11: Peak Collector Current versus Duty Cycle

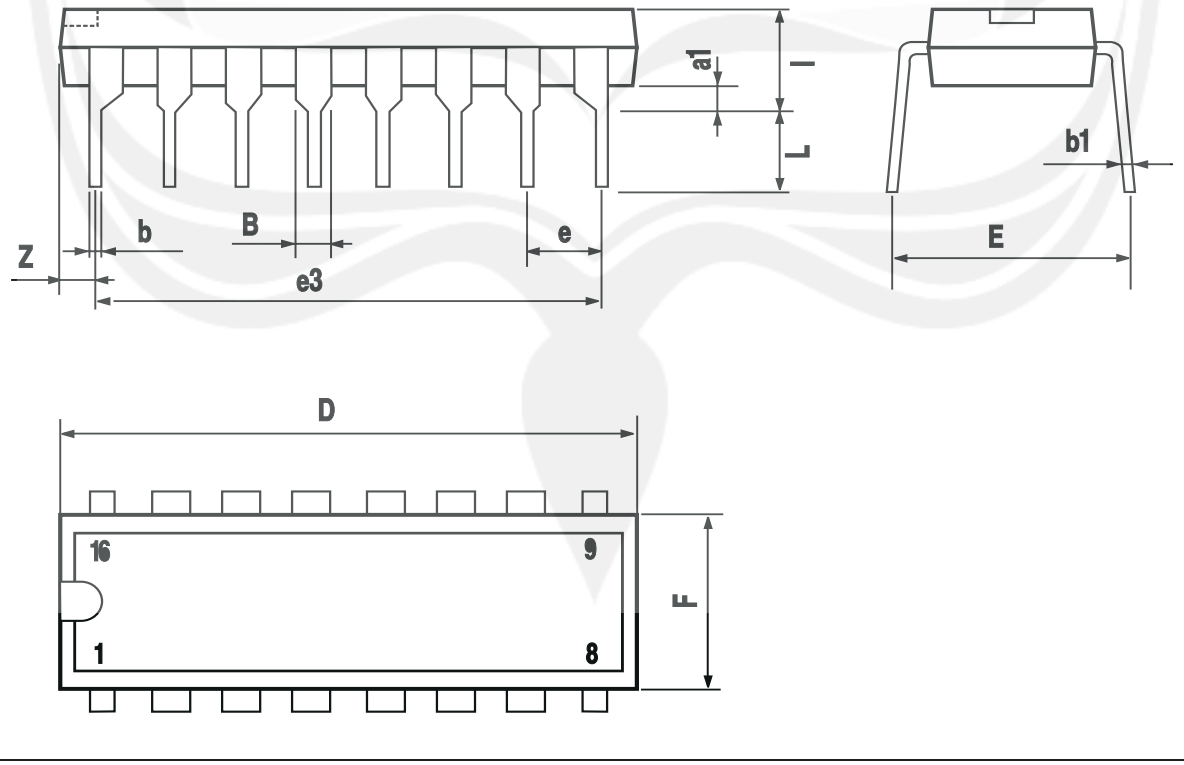


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050

OUTLINE AND MECHANICAL DATA

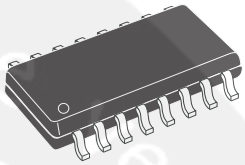


DIP16



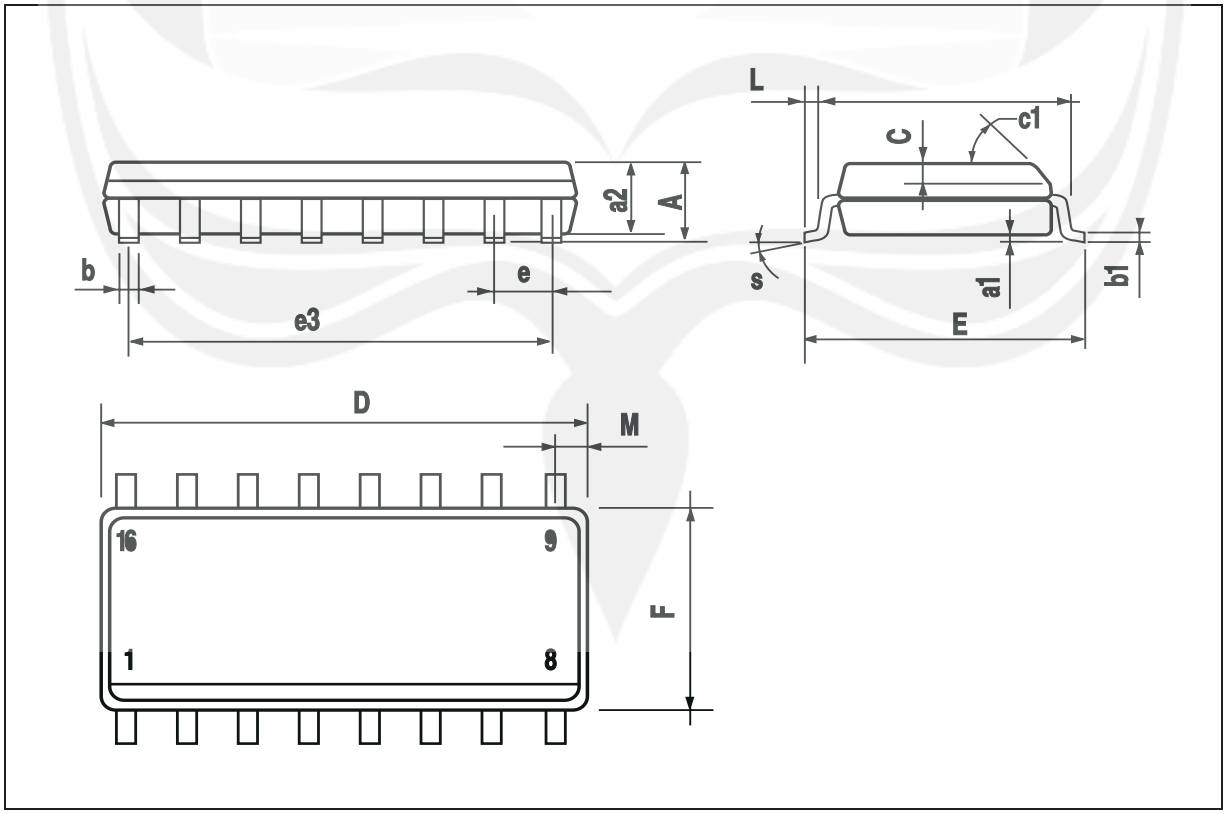
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.069
a1	0.1		0.25	0.004		0.009
a2			1.6			0.063
b	0.35		0.46	0.014		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.020	
c1	45˚ (typ.)					
D (1)	9.8		10	0.386		0.394
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F (1)	3.8		4	0.150		0.157
G	4.6		5.3	0.181		0.209
L	0.4		1.27	0.016		0.050
M			0.62			0.024
S	8˚(max.)					

OUTLINE AND MECHANICAL DATA



SO16 Narrow

(1) D and F do not include mold flash or protrusions. Mold flash or potrusions shall not exceed 0.15mm (.006inch).



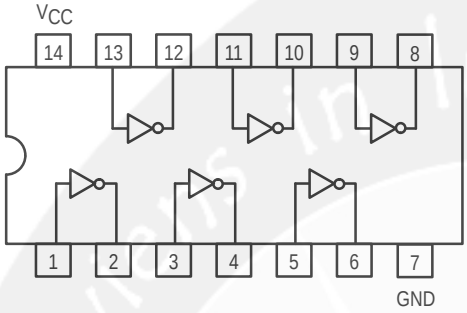
MOTOROLA

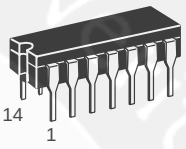
HEX INVERTER

SN54/74LS04

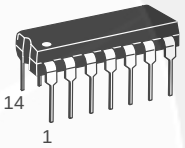
HEX INVERTER

LOW POWER SCHOTTKY

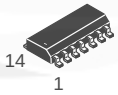




J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06



D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	–55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			–0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current (Note 1)		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current Total, Output HIGH				2.4	mA	V_{CC} = MAX	
	Total, Output LOW				6.6			

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
t_{PLH}	Turn-Off Delay, Input to Output		9.0	15	ns	V_{CC} = 5.0 V C_L = 15 pF
t_{PHL}	Turn-On Delay, Input to Output		10	15	ns	